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JAN 80 J G BOUCHARD, J A BRADY, B T JOYCE DAAG39-78-C-0002

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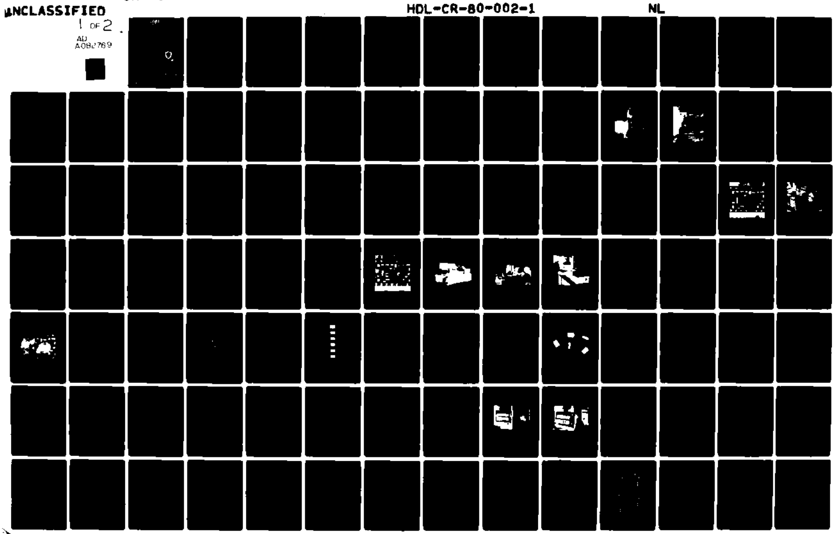

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INTERFACE CIRCUIT 11726909
MATERIALS, METHODS, AND TECHNOLOGY PROGRAM

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Prepared by RCA Corporation
Government Systems Division
Automated Systems
Burlington, MA 01803

Under contract DAAG-39-78-C-0002

U.S. Army Electronics Research
and Development Command
Harry Diamond Laboratories
Adelphi, MD 20783

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This report summarizes a materials, methods, and technology program associated with a hybrid microelectronic, special-purpose interface circuit for use in the M587 and M724 Electronic Timing Fuzes. The pilot production phase of this 4-phase program provided operation rates and yield data necessary to make realistic cost estimates of high-volume production of this hybrid. To help reduce production costs, this hybrid interface circuit employs a custom-

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20. ABSTRACT (Cont'd)

designed monolithic integrated circuit. Transfer molding packaging techniques were developed to meet demanding environment requirements that include 30 KG mechanical shock.

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1. INTRODUCTION

This materials, methods, and technology (MM&T) program provided for the design, development and fabrication (through a pilot production run) of a special purpose hybrid interface circuit to be employed in the M587 and M724 Electronic Timing Fuzes for the Harry Diamond Laboratories (HDL), Adelphi, MD. Originally, this effort was to be in conformance to Source control drawing (SCD) 10990455 (since modified to SCD 11726909).

This final technical report is written in response to contract DAAG39-78-C-0002 dated 31 October 1977, statement of work (SOW), paragraph F.9.6, contract data requirements list (CDRL) sequence A007, and in compliance with contract modifications P00001 through P00010 dated 2 January 1980.

The contract change status is per table I as follows:

TABLE I - CONTRACT CHANGE STATUS

Effective Date		Description
10/31/77	DAAG39-78-C-0002	Contract/Award
11/29/77	Mod. P00001	Distribution/Payment Changes
1/9/78	Mod. P00002	Funding Changes
1/9/78	Mod. P00003	Delete P00002/Funding Changes
6/9/78	Mod. P00004	Schedule Change
6/20/78	Mod. P00005	Schedule Change
7/19/78	Mod. P00006	Amend P00003, Correct P00005
3/6/79	Mod. P00007	Add Special Test Equipment
3/20/79	Mod. P00008	Source Control Drawing Change
5/14/79	Mod. P00009	Schedule Change
1/2/80	Mod. P00010	Schedule and Delivery Change

This MM&T effort was expended in four phases:

- Phase I: Design Evaluation
- Phase II: Engineering Samples
- Phase III: First Article Acceptance Sample (FAAS)
- Phase IV: Pilot Production Run

Phase I: The design evaluation phase was completed. The final version of the phase I report stating the results and the accomplishments of this effort was submitted on 31 December 1978 per SOW paragraph F.6.4 and CDRL sequence A003. A summary of this effort is provided in section 2.1 of this final technical report.

Phase II: The engineering samples phase was completed. The final version of the phase II report stating the results and the accomplishments of this effort was submitted on 1 February 1979 per SOW paragraph F.7.5 and CDRL sequence A005. A summary of this effort is provided in section 2.2 of this final technical report.

Phase III: The FAAS phase was completed. The results and the accomplishments of this effort were submitted as the FAAS report on 1 December 1978 per SOW paragraphs F.8.2 and F.8.5 and CDRL sequence A006. A summary of this effort is provided in section 2.3 of this final technical report.

Phase IV: The pilot production run is complete. The results and the accomplishments of this effort are submitted herewith per SOW paragraph F.9.6 and CDRL sequence A007. The documentation of this effort is provided in section 2.4 of this final technical report.

2. PROGRAM HISTORY

To facilitate relating the accomplishments to the program objectives, the history of the accomplishments is presented by phases and as much as possible in the same sequence as the SOW.

2.1 Phase I: Design Evaluation

In phase I, all preparatory activities were conducted to prepare the circuit and process for engineering sample fabrication. The circuit design was optimized to eliminate false triggering and provide safety margins at extreme temperatures. A manufacturing flow chart was generated and submitted, and an extensive materials evaluation effort was conducted to find the appropriate molding material. This report provides the pertinent information relative to the efforts of phase I.

2.1.1 Design Optimization

The need for changes in the baseline design was recognized in a previous contract (DAAG39-76-C-0146) and implemented in phase I of this contract. These changes were required to provide proper operation of the interface circuit at all specified temperatures and to provide immunity to system noise spikes. These changes inv lved alterations of the circuit design, the chip design, the substrate layout, and ultimately a new SCD 11726909. An analysis of the molding configuration was also performed to verify its thermal expansion compatibility.

Circuit Design: The control-line circuits were modified to prevent false triggering caused by noise pulses generated in the system mock-up tester. This malfunction was not observed in the standard hybrid testing as no noise immunity test is specified in the hybrid SCD. The problem was resolved by reducing the base-to-emitter and series resistors on the thick-film substrates rather than in the custom integrated circuit (IC) chip.

Integrated Circuit Chip Design: The two resistors related to the control-line circuits were deleted from the IC chip. In addition, the test circuit for the IC chip was modified to provide guard-banded operation and to assure proper operation at extreme temperatures. The choice of guard banding rather than specifying high and low temperature limits and the choice of modifying the test circuit rather than changing the test conditions were made in the interest of maintaining a low cost.

Hybrid Layout: The addition of two resistors had a very significant impact on the substrate layout as space was very limited prior to the addition of these two resistors. A protracted effort was conducted to find the space required for the resistors. Some space was saved by reducing the size of the chip capacitor (also reducing its cost), and the balance of the required space was made available by a more judicious layout. The revised layout has larger wire bond pads to enhance the automatic wire bonding capability.

The resulting layout permitted the use of jumper wires for this contract, yet retained the ability to convert to thick-film crossovers when the volume develops to a point where crossovers will be more cost-effective than jumper wires. This concept allows for optimum cost-effectiveness at all quantity levels.

2.1.2 Manufacturing Information

A series of manufacturing flow charts identifying operations, materials, and basic conditions was generated and reviewed with the customer. Although this chart listed RCA process specifications that are not deliverable as part of this contract, it identified the generic materials and basic conditions enabling anyone knowledgeable in thick-film state of the art to reproduce this circuit.

A very comprehensive cost estimate was performed by using an existing Hybrid Scheduling Computer Program. All details of the information required and entered in this program were provided. Cost estimates were generated by using estimated rates for processes to be demonstrated and projected high-volume automated-line rates. These estimates were generated for various levels of efficiency and yield factors to cover the extremes anticipated for this process and circuit.

A complete list of the estimated operation rates for both the demonstrated and the high-volume line was provided as well as a tabulation of the unit-cost breakdown.

2.1.3 Materials Evaluation

RCA made use of its extensive plastics and plastic-molding experience at its Solid State Division (SSD) in Somerville, NJ, as well as the hybrid expertise of the prime contractor at Automated Systems (AS), at Burlington, MA.

A special single-cavity mold was designed and fabricated to explore the materials molding problems. This was a frontier. To the best of our knowledge, this is the first true transfer molding of a hybrid microcircuit in a lead frame. There are several commercial resistor and capacitor networks molded in this configuration, but these are not true hybrids as they do not have semiconductor and capacitor chips or wire bonds. Furthermore, they are on a 300-mil dual-inline row spacing, not the 600-mil spacing of this unit. This program has added new technology to this relatively uncharted but promising area.

This materials evaluation was the major effort during phase I. Ten materials were used to fabricate approximately 130 samples. Two of the materials exhibited properties which appeared to be satisfactory for this application, namely, Dow Corning 307 (silicone) and Hysol MH8F (epoxy).

All samples which showed promise after molding were temperature cycled to establish that the solder joints were sufficiently strong and to evaluate the thermal matching of the materials. To evaluate the strength of the wire bonds, wire bridges, and chip attachments, a group of units (test specimens) with chips and wire bonds was fabricated and evaluated. After successfully passing temperature cycling, constant acceleration, and air-gun tests, the test specimens were shipped to HDL on 26 June 1978.

2.1.4 Report (Phase I)

The final version of the phase I technical report was submitted on 31 December 1978.

2.2 Phase II: Engineering Samples

The engineering samples phase was beset by several problems which caused substantial schedule slippage. The most serious problem was the bond wire breakage during molding. This forced a complete rebuilding to replace the first engineering sample lot. This problem was completely unforeseen. In fact, even when it had occurred, we still had hopes of eliminating it by simply raising the molding temperature. Hopefully, this would reduce the viscosity of the molding compound and solve the problem. That was not to be.

We now realize that we were dealing in a frontier element of transfer molding (the molding of relatively large ceramic substrates). Realistically, we should not have been surprised that we encountered this problem; we were in relatively unexplored, uncharted areas. Fortunately, a solution was immediately found, and the only lost time was that required to rebuild the engineering sample lot.

2.2.1 Manufacturing Information

A second engineering sample lot was manufactured because of the fact that test revealed damaged wire bonds caused by molding of the first engineering sample lot. The plastics experts had expected that an increase in molding temperature would decrease viscosity of the plastic sufficiently to fully eliminate damage to wire bonds. Thus, the second lot was subdivided into two halves. The first half used 95-5 Sn-Pb solder paste to allow increasing the mold temperature from 160°C to 177°C, which is recommended by Dow Corning. The other half used 62-36-2 Sn-Pb-Ag as did the damaged lot, to be molded at 160°C. To prevent wire damage in molding of the lot using the lower temperature solder, the wires as well as the semiconductors were coated with an epoxy - Hysol 4228.

The higher molding temperature did not prove successful - the bond wire damage problem continued as severe as in the lower temperature trial. The epoxy coated second lot was successful, and the 25-piece engineering sample was fabricated in this manner. The number of starts and the yield to the end of each process step are shown in table II.

TABLE II - ENGINEERING SAMPLE YIELD SUMMARY - PHASE II

Operation	Quantity					Yield (%)	
	Start	Setup	Net	Reject	Accept	Oper.	Start
Substrate Fab	81	0	81	14	67	82.7	82.7
Resistor Trimming	67	0	67	7	60	89.6	74.1
Hybrid Assembly	60	10	50	0	50	100.0	74.1
Molding	50	0	50	0	50	100.0	74.1
Final Elect. Test	50	0	50	18	32	64.0	47.4
Final Elect. Test*	50	0	50	10	40	80.0	59.3

*Includes all units that passed all parameters except IR45.

The substrate fabrication and the resistor trimming yield were lower than those obtained in the previous contract. On the current contract, we have converted to the use of a 4 x 5 matrix 20-image scored alumina substrate in place of the single-image substrate in use previously. The productivity increased by almost the same factor. The attendant yield shrinkage is more than offset by the gain in productivity. During hybrid assembly, 10 units were consumed to establish resistor trimming values that center the regulation voltage and set the initialization threshold voltage; thus, they were not counted as a loss.

The degree of survivability of the plastic-ceramic-lead frame system was evaluated by extending the number of temperature cycles well beyond the specified limits.

The firing circuit conductors were made especially wide and as short as possible to reduce the series resistance and maximize the energy throughput. This was a point covered during a layout review with HDL.

A technique for adjusting the regulation voltage and the initialization threshold voltage was established. Because of the tolerances in integrated circuit processing, these parameters may vary from lot to lot. The spread of the voltage parameters in a given lot is usually within the specified limits, but the average value from lot to lot may differ from the desired value by an amount sufficient to

require correction by trimming external resistors on the ceramic substrate.

The substrate resistors are all pretrimmed, including R15, R16, R10, and R11, as specified by the trimmed substrate drawing 11726765. Then a sample of thirteen units is fabricated and assembled with chips from each lot of integrated circuits. These units are tested and the average value for the initialization circuit threshold voltage are determined for each integrated circuit lot sampled. These average values are then used to establish which resistors must be retrimmed and to what values they must be trimmed. Retrimming is then performed on substrates in quantities appropriate to the sizes of the lots of associated integrated circuit chips.

Regulation Voltage Control: The regulated output voltage is measured between hybrid pins 10 and 4. If the measured average value, V_O, is smaller in magnitude than 23 volts, R16 should be trimmed to a value established as follows:

$$R16 = \frac{30R}{30 - R} \qquad \text{in kilohms}$$

$$\text{where} \qquad R = \frac{836}{V_O} - 12.75$$

If the measured average value is larger in magnitude that 24.4 volts, R15 should be trimmed to a value established as follows:

$$R15 = \frac{17R}{17 - R} \qquad \text{in kilohms}$$

$$\text{where} \qquad R = 22.5\ V_O/(65.53 - V_O)$$

Initialization Threshold Voltage Control: The initialization threshold voltage is that input voltage applied between hybrid pins 11 and 4 which causes the output voltage at pin 5 to switch from a low level to a high level. If the threshold voltage is between -19.0 volts and -20.0 volts, no correction of either R10 or R11 is necessary.

If the magnitude of the threshold voltage, V_T, of the sample is smaller that 19.0 volts, R11 should be trimmed to decrease the sensitivity of the circuit. The trimmed value is found by using the following equation:

$$R11 = 40\ \frac{42.41 - V_T}{V_T} \qquad \text{in kilohms}$$

If the magnitude is greater than 20.0 volts, the circuit is not sensitive enough and R10 must be trimmed. The trimmed value is found by using the following equation:

$$R10 = 47 \frac{V_T}{42.41 - V_T} \quad \text{in kilohms}$$

2.2.2 Testing/Test Results

The effort required to test the engineering sample was greatly reduced by the adaptation of one of RCA's AN/USM-410 test systems. The time of test and the data collection time was lowered by more than 3:1 when compared with manual procedures.

As shown in table II, the group A electrical yield was 64 percent to the specification existing at that time. Most of the failures were to a specification which was subsequently changed (IR45)*, and the yield was 80 percent to the modified specifications.

The statistical information on all parameters (the mean, sigma, median, low limit and high limit) is provided by table III.

A plan to conduct the group B environmental test in an order supplying the most useful information was developed and submitted to HDL for approval. This plan was approved, and the group B testing was performed accordingly in the following sequence:

Subgroup	A2	25°C performance	25 units
	A3	71°C performance	25 units
	A4	-50°C performance	25 units
	B1	temperature cycling	25 units
	B3	constant acceleration	25 units
	B2	mechanical shock	12 units
	B4	high temperature storage	13 units

Only one unit failed in these tests. This unit failed in temperature cycling (the regulator output voltage increased catastrophically from 24.09 to 46.04 V).

*IR45 changed:

	Max	Min	Test Voltage
From	-1.16	-1.30	-27 VDC
To	-0.42	-0.49	-10 VDC

TABLE III - ENGINEERING SAMPLE DATA SUMMARY - PHASE II

Parameter	Sigma	Specs. Low Limit	Measured Low Limit	Mean Value	Median Value	Measured High Limit	Specs. High Limit
IR16	-	1.6	2.02	2.02	2.02	2.02	2.4
IR10	.10	6.1	7.12	7.42	7.43	7.72	8.0
IR3	0.030	0.77	0.793	0.883	0.890	0.973	1.03
IR14	0.06	0	1.13	1.19	1.17	1.25	1.6
+VP	0.022	28.9	29.02	29.09	29.09	29.15	29.7
IR6	0.015	0.39	0.410	0.455	0.460	0.500	0.53
V12	-	0	0	0	0	0	0.1
-VP	0.015	28.5	29.02	29.07	29.07	29.11	29.7
IR45*	0.020	1.16	1.196	1.256	1.260	1.366	1.30
V2A	-	0	0	0	0	0	0.2
V2B	.070	7.4	9.25	9.49	9.50	9.70	13.0
V1A	-	2.3	2.42	2.43	2.42	2.43	2.6
V1AD	-	1.1	1.32	1.33	1.32	1.33	1.7
VR39	-	0.47	0.56	0.57	0.56	0.57	0.66
V1B	0.023	14.1	15.25	15.32	15.32	15.39	15.6
V1BD	-	1.4	1.69	1.67	1.67	1.65	1.8
IR42	-	0.21	0.28	0.28	0.28	0.28	0.38
IR8	0.085	2.0	2.44	2.70	2.72	2.95	5.85
V11A	0.480	21.8	21.91	23.35	23.40	24.79	25.6
V10A	0.475	22.2	22.81	24.23	24.25	25.66	26.0
V13A	-	0	0	0	0	0	0.1
V11B	.012	25.8	25.97	26.00	26.00	26.04	26.8
V8A	-	0	0	0	0	0	0.1
V5A	-	0	0	0	0	0	1.0
V5B	-	11.0	12.19	12.46	12.47	12.73	14.0
V5C	-	0	0	0	0	0	1.0
V5D	0.264	11.0	11.74	12.45	12.58	13.33	17.0
T5A	16.1	0	10.3	31.8	25.0	80.0	200.0
T5B	2.0	10	28.8	34.8	35.0	40.8	100.0
V7A	-	0	0	0	0	0	0.5
V8B	0.013	16.8	16.94	16.98	16.98	17.02	17.1
V7B	0.210	12.0	13.39	14.02	14.00	15.28	17.1
V7C	1.095	12.0	19.86	23.14	23.40	26.43	26.1

*Selected lot.

2.2.3 Manufacturing Methods Notebook

A notebook compiling all drawings, specifications, process descriptions, and inspection criteria required to manufacture the interface circuit was prepared. This notebook was kept current and made available for review by the customer. The exact process used for the 25 unit engineering sample was documented on the traveler kept in this notebook.

2.2.4 Changes

The only deficiency discovered during phase II was test related, IR45. The only purpose for this test is to measure the resistance value of R45, identified as R17 in the new schematic for the circuit. The specified test voltage was -27 V, which in some cases exceeded the breakdown voltage of a reversed bias semiconductor junction which caused a shunt current and a pseudo-low resistor. This problem was subsequently resolved with a specification change for a test voltage of -10 V instead of -27 V.

2.2.5 Report (Phase II)

The final version of the phase II report was submitted on 1 February 1979 and included all information requested in the SOW, except for the analysis of the single environmental test failure.

There was no change of the unit cost from that presented in the phase I report. But an analysis was initiated to determine the appropriate lot size, man loading needs and equipment needs.

In addition to the information required by the SOW, this report included the following:

a) A summary of the tooling effort and the drawings generated in this phase.

b) A revised schematic reflecting the optimized design for the custom IC chip. Up to this point, the official schematic still described the multichip version of this circuit.

c) A discussion and a tabulation of necessary changes in specification (at this time, deviations) resulting from this contract.

d) A theoretical stress analysis of the plastic-ceramic package design.

2.3 Phase III: First Article Acceptance Sample

As required by contract, over 700 devices were fabricated, and 174 were randomly selected and subjected to the FAAS tests called out in the original SCD 10990455.

2.3.1 Manufacturing Information

The manufacturing quantities and the yield data for phase III are tabulated in table IV.

TABLE IV - MANUFACTURING QUANTITY AND YIELD DATA - PHASE III

	1st Elec. Test		Rework Elec.Test		Mold		Final Elec.	
	Start	Accept	Start	Accept	Start	Acc.	Start	Acc.
Operational Quantity	834	709	125	106	815	815	815	705
Operational Yield (%)	-	85.0	-	84.8	-	100.0	-	86.5
Yield from Start (%)	-	85.0	-	-	97.7	97.7	97.7	84.5

An analysis of the failure distribution at rework after the first electrical test was performed to determine the causes of yield shrinkage. The distribution of failures as a percentage of the total rework quantity is tabulated in table V.

TABLE V - REWORK FAILURE DISTRIBUTION - PHASE III

Failure	Distribution Percentage (%)
Silicon-Controlled Rectifier (SCR) only	22
Integrated Circuit (IC) Only	51
Both SCR and IC	11
Marginal	16

The IC was associated with at least 62 percent of the failures at the first electrical test.

2.3.2 Testing/Test Results

Comparison Sample: The 25 unit phase III comparison sample was completed and submitted to HDL on 7 November 1978.

Acceptance Sample: The 158 unit phase III acceptance sample was completed and submitted to HDL on 1 December 1978.

Subgroup C1 - Gunfire Failure Analysis: All 25 acceptance test subgroup C1 - gunfire test specimens were returned to RCA/AS after gunfire for end-point testing. All units were subjected to end point retest and five units failed. In all five failures, it was one of the front units of the four unit encapsulated test specimen that failed. Each encapsulated test specimen was cut in half longitudinally, and the encapsulation was chemically removed from the failed interface circuit. An overall view of the failed unit (as described) is provided in figure 1. A close-up view of the same unit is provided in figure 2. In each figure, the serial number of the failed unit shown is 134 (HDL I9). Failure analysis data is provided in table VI.

Figure 1. Subgroup C1 Gunfire Test Specimen

Figure 2. Subgroup C1 Gunfire Test Specimen Close-up

TABLE VI - SUBGROUP C1 FAILURE ANALYSIS DATA - PHASE III

HDL No.	Serial No.	V11B	V5B	V5D	T5A	T5B	Capacitor
I9	134				0	0	Missing
I11	136				6	0	Missing
I13	138	-0.86	-0.01	-0.01	0	0	Present
I17	142				6	0	Missing
I19	144				0	0	Missing

During the end point retest prior to removal of the encapsulant, variables data for the T5B failures were symptomatic of an open capacitor. This was confirmed upon chemical removal of the encapsulant for four of the units.

One device, S/N 138, apparently did not suffer capacitor separation, but did suffer other unidentified damage.

Chemical removal of the encapsulant is a time-consuming, inexact process which requires agitation of the specimen in a chemical solution. The missing capacitors were found to be unattached to the substrate. It is reasonable to assume that the shock of gunfire (especially on the forward units) was sufficient to open the solder bond between the capacitor and substrate. Evidence of inadequate solder joints and leaching was also indicated. This degradation of the solder joint was possibly caused by the lead frame to substrate reflow solder processes that have been changed for phase IV production from a furnace to a hot plate process. We anticipate that the phase IV subgroup C1 gunfire end point testing will confirm our conclusions. In addition, it would be advisable to provide additional attention to these solder joints during future production and to epoxy encapsulate the capacitor along with the other components (before transfer molding) for additional strength and protection. This was not accomplished during phase IV as this phase III failure analysis was not concluded until after the phase IV units were molded.

The before and after variables data for the phase III acceptance test subgroup C1 gunfire test specimens is provided in appendix A.

2.4 Phase IV: Pilot Production Run

Phase IV, per contract SOW paragraph F.9.1, was to consist of a total lot quantity of 2000 hybrid interface circuits, SCD 11726909). A comparison sample quantity of 25 units was to be randomly selected and supplied immediately upon completion to HDL. An acceptance test sample of 174 units was to be randomly selected from the pilot production run of which 158 units were to be subjected to electrical testing and 16 units were to be subjected to mechanical testing.

2.4.1 Manufacturing Information

Introduction: The completion of phase IV can be considered as taking place in a simulated mass production atmosphere in various orderly and functional activities as follows:

Substrate fabrication
- Substrate preparation (Vendor)
- Thick-film processing (RCA/AS)
- Resistor trimming (RCA/SSD)

Hybrid assembly
- Substrate assembly (RCA/AS)
- First electrical test and inspection (RCA/AS)
- Substrate assembly rework (RCA/AS)
- Encapsulation (RCA/AS)
- Lead frame assembly (RCA/AS)
- Transfer molding (RCA/SSD)
- Mold reject reevaluation (RCA/AS)
- Marking (RCA/AS)
- Final electrical test and inspection (RCA/AS)

Packaging and Shipping (RCA/AS)

However simple and orderly that production process may seem, all manner of diversionary activities took place in this basic in-line production flow process. To appropriately disclose the events that took place, these activities are presented in the indicated order, primarily to provide the appropriate operational sequence of events.

Process Flow Chart: To aid in understanding the content of this report, a 16 sheet process flow chart is provided to graphically illustrate the operational production sequence. Rather than supplying this chart as an appendix to this report, we have chosen to include the pertinent sheets of the process flow chart as an integral part of the text at the point where the operations displayed in the chart are discussed.

Product Illustrations: In addition, photographs of the units are provided at various stages of the manufacturing process. These photographs are also included in the text at the points where the illustrations are most appropriate.

Lot Formation: To provide an overview of phase IV, it must be recognized that totally different operational functions are accomplished in providing interface circuit SCD 11726909. To relate these operational functions, various lots and subdivisions of these lots were formed. A graphical illustration of the interrelationship of these lots is provided in figure 3.

The thick-film processing (printing, drying, and firing of the thick-film materials on the alumina substrate) was accomplished in one lot. Since the resistors had to be trimmed to match two lots of IC chips, two substrate resistor trimming lots (B1 and B2) were formed from the substrate fabrication lot.

Initially, two lots (not shown) were formed for substrate assembly to match the two substrate resistor trimming lots (B1 and B2). For expediency in subsequent assembly operations, these initial two substrate assembly lots were subdivided into substrate assembly sublots. Lot B2 was subdivided into four substrate assembly sublots HD001 through HD004, and lot B1 was subdivided into substrate assembly sublots HD005 and HD006. At first electrical test, it was determined that a wire bonding problem existed, and the first electrical test rejects from all substrate assembly sublots HD001 through HD006 were formed into a seventh substrate assembly rework sublot HDR01. Each of the six substrate assembly sublots HD001 through HD006 was fully segregated. However, within the seventh substrate assembly sublot HDR01, no segregation was provided.

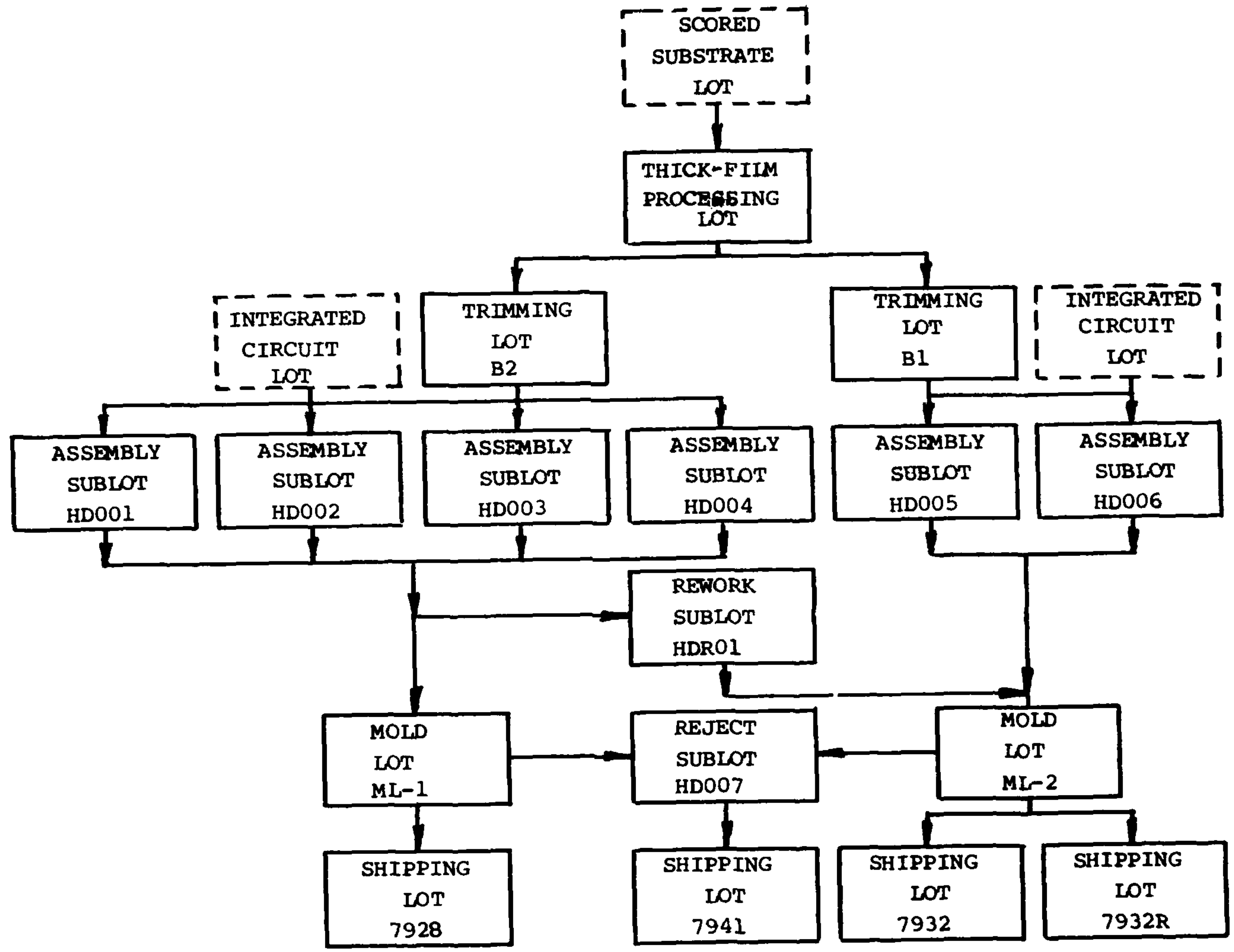


Figure 3. Interface Circuit, Phase IV - Lot Formation Diagram

All of the acceptable units from the seven substrate assembly sublots were combined into two mold lots. Mold lot 1 (ML-1) was formed from the acceptable units of substrate assembly sublots HD001 through HD004. Approximately a month later, mold lot 2 (ML-2) was formed from the acceptable units of substrate assembly sublots HD005, HD006, and HDR01. All substrate assembly sublots were segregated during molding.

All of the acceptable units from ML-1 were identified with the date code 7928, and all of the acceptable units from ML-2 were identified with two date codes - 7932 for sublots HD005 and HD006 and 7932R for sublot HDR01. Unacceptability was determined by notches put in the lead frame by RCA/SSD.

All of the units rejected as a result of molding were set aside as unsegregated SSD mold rejects. At a later date, these SSD mold rejects were formed into SSD mold reject sublot HD007 and reevaluated. Upon reevaluation, many of these units were found to be acceptable and were identified with date code 7941.

Upon completion of production, four shipping lots of acceptable interface circuits were available for shipment (7928, 7932, 7932R and 7941). The comparison sample was drawn from lots 7928 and 7932. The acceptance sample was drawn from lot 7932. The phase IV balance of lots 7928, 7932, 7932R and 7941 was also shipped. Shipping lot numbers and date codes are synonymous.

Program Problem Area Summary: In the course of the pilot production run processing, five basic problem areas arose that require some understanding as follows:

Inadequate wire bonding operations

Program manager loss and changeover

Known mechanical rejects (red leads)

SSD mold rejects versus mold void rejects

Incomplete record keeping

Each of these problem areas is a separate entity. However, because they are all associated with each other, the temporary lack of program coordination was compounded.

Production was progressing in a normal way in conformance with the program plan until wire bonding of the chips to the substrate conductors was started. It was discovered during the automatic wire bonding demonstration with the contracting office's representative in attendance that inadequate wire bonds to the thick-film gold pads were being made. A representative production process was impossible to demonstrate. After examination, the conclusion was drawn that either the thick-film gold was too thick, soft, or contaminated by previous operations. A simple rework operation was initiated to eraser burnish the thick-film gold pads so that processing could continue. Automatic wire bonding was again initiated, and the problem apparently had been solved as adequate wire bonds were obtained. Our success was short-lived. First electrical test proved disastrous. Upon examination of failed units, it was discovered that, in our efforts at a simple solution, we had created additional problems. Insufficient attention had been given to the rework eraser burnishing in our attempt to expedite the production effort and the automatic wire bonding demonstration. The surfaces of many of the semiconductor chips (in particular, the custom IC) had been scratched during the rework burnishing operation, causing electrical malfunctions. Unfortunately, the glass passivation of the chip surface (normal to IC processing) had been omitted by the vendor on the custom IC's, allowing them to be more vulnerable to this type of damage. Our problem had been unwittingly compounded. Eventually, all 395 eraser burnished units were formed into sublot HDR01 to be candidates for component replacement.

During this period, the program manager accepted employment with another firm, and a new program manager was appointed. Although each individual associated with the program carried out his responsibilities in proper fashion, each was concerned only with his own sphere of influence so that, at a critical period of the production process, program coordination was lacking.

There were known mechanical rejects identified with red leads that were intentionally allowed to remain in the production process for experience. However, communications were poor during management changeover, and the significance of the red leads was lost, contributing to inadequate record keeping. Eventually, this problem was reidentified. However, the records can be only loosely established.

Toward the end of the management changeover, during the transfer molding at RCA/SSD, it was determined that improved mold yields could be gained by providing additional mold relief through lead frame carrier modification. RCA/SSD clipped the lead frame longitudinal carrier at certain mold cavities. It had been inadvertently assumed that this clipping indicated an SSD mold reject. There were 207 units so designated. In addition, there were 60 actual mold void rejects. Eventually, the so-called SSD mold rejects were identified as potentially acceptable units and were formed into mold reject reevaluation sublot HD007.

With all of these conditions, it is not difficult to see that the majority of attention is paid to acceptable units during production. Once a unit is rejected, little attention is expended on its behalf. This is normal and understandable. However, with all of the rejections, it is not hard to understand that incomplete records are the attendant result. During the balance of this final report, the data submitted is based on the records as they stand with minor modifications where they are clearly obvious. Where adjusted data is provided, it is clearly indicated.

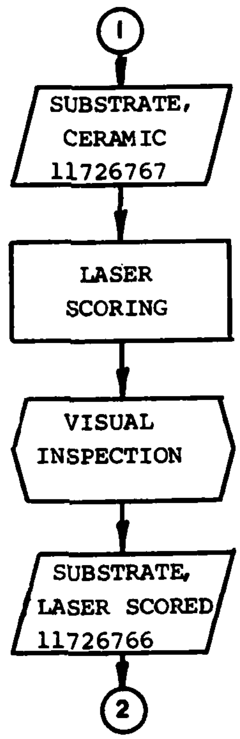
Copies of the phase IV process travelers for the four shipping lots (date codes) are provided in appendix B. For an in-depth review of the activities and the conditions that existed at various stages of production, refer to the appropriate sections of the text.

Substrate Preparation: These are the activities (flow chart 1) necessary to prepare the alumina substrate for screen printing of the interface circuit.

The thick-film substrate is a 3 x 3 x 0.025 in. thick alumina plate laser scored in a four by five circuit area matrix to provide 20 interface circuit thick-film substrates per substrate plate.

Note: The 20 interface circuit thick-film substrate plate is retained throughout subsequent substrate fabrication operations until snapped into individual thick-film substrates for resistor trimming.

The substrate laser scored SCD 11726766, was purchased complete from Laser Services, Inc., North Billerica, MA. A quantity of 221 plates with 4420 circuits was available for subsequent processing.



Flow Chart 1. Substrate Preparation

There are no unique requirements in the preparation of alumina substrates for subsequent fabrication operations. However, refer to paragraph 5.1.

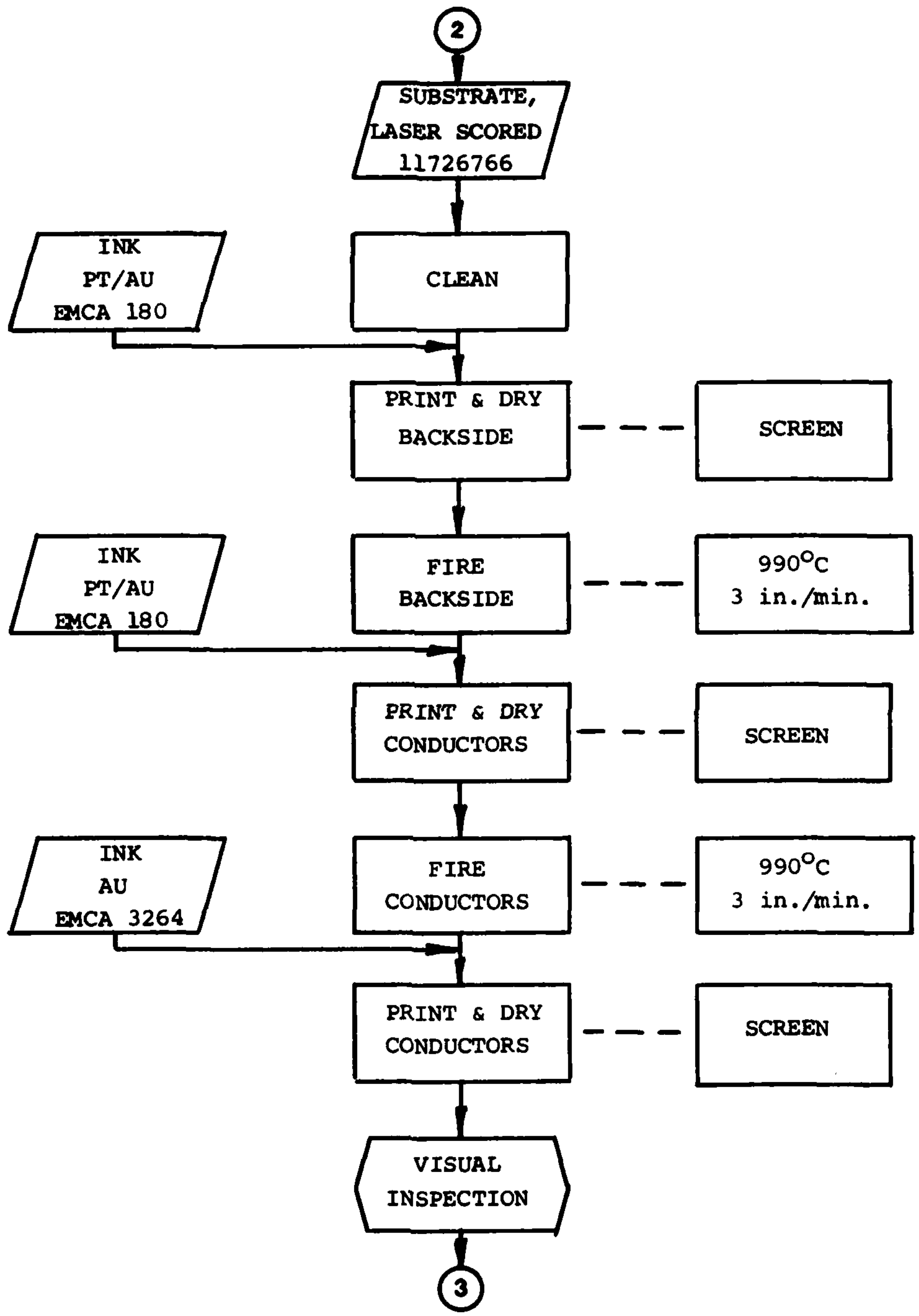
Thick-Film Processing: These are the substrate fabrication operations associated with thick-film processing (flow charts 2 to 5) necessary to print, dry, and fire conductors, resistors, and glaze on the thick-film substrate, laser scored SCD 11726766, in preparation for subsequent resistor trimming and hybrid assembly. Units are processed in multiples of 20. A photograph of the thick-film substrate plate prior to individual circuit separation is provided in figure 4. An individual separated-circuit photograph is provided in figure 5. A photograph of the integrated printer and the dryer system is provided in figure 6.

On 2 November 1978, the interface circuit SCD 11726909 was physically started at RCA/AS, on phase IV with the start of thick-film processing.

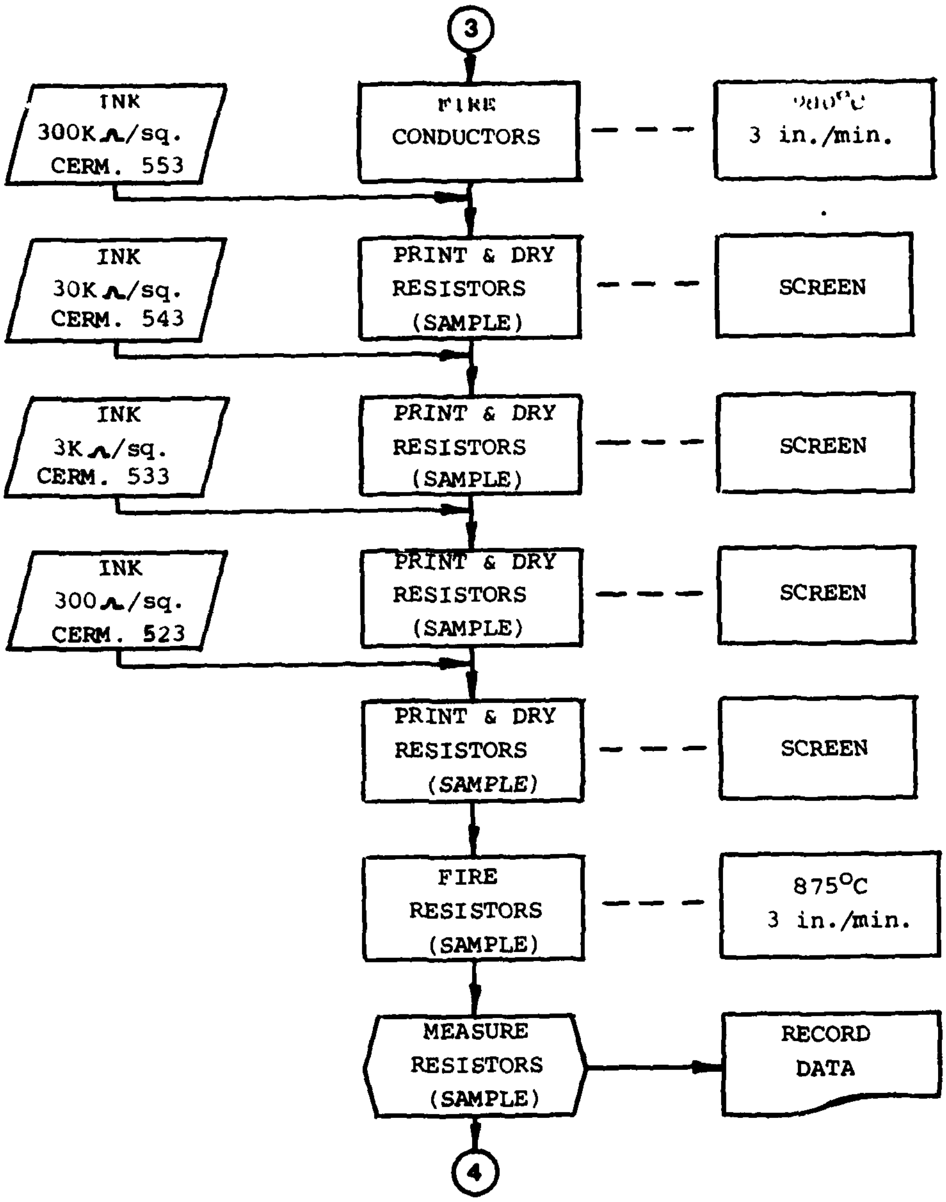
Two hundred twenty-one laser-scored substrate plates composed of 20 units each (a total of 4420 interface circuits) were started at RCA/AS. Two plates (40 circuits) were consumed prior to fabrication as conductor setup samples. Four plates (80 circuits) were consumed as resistor setup samples. A quantity of 786 units was rejected during thick-film processing and separation into individual units. Rejections during thick-film processing were marked for subsequent rejection upon separation. The rejections were caused primarily by faults in the printing process and breakage at separation. Some of the faults in printing are the result of deviations from flatness on the alumina substrate.

The acceptable balance of 3514 units was completed on 9 February 1979. Exclusive of the six substrate fabrication setup plates for 120 circuits, the basic net start quantity was 4300 units. The yield from thick-film processing operations was 81.7 percent. Since this was the start of operations, the yield from net start was identical, 81.7 percent.

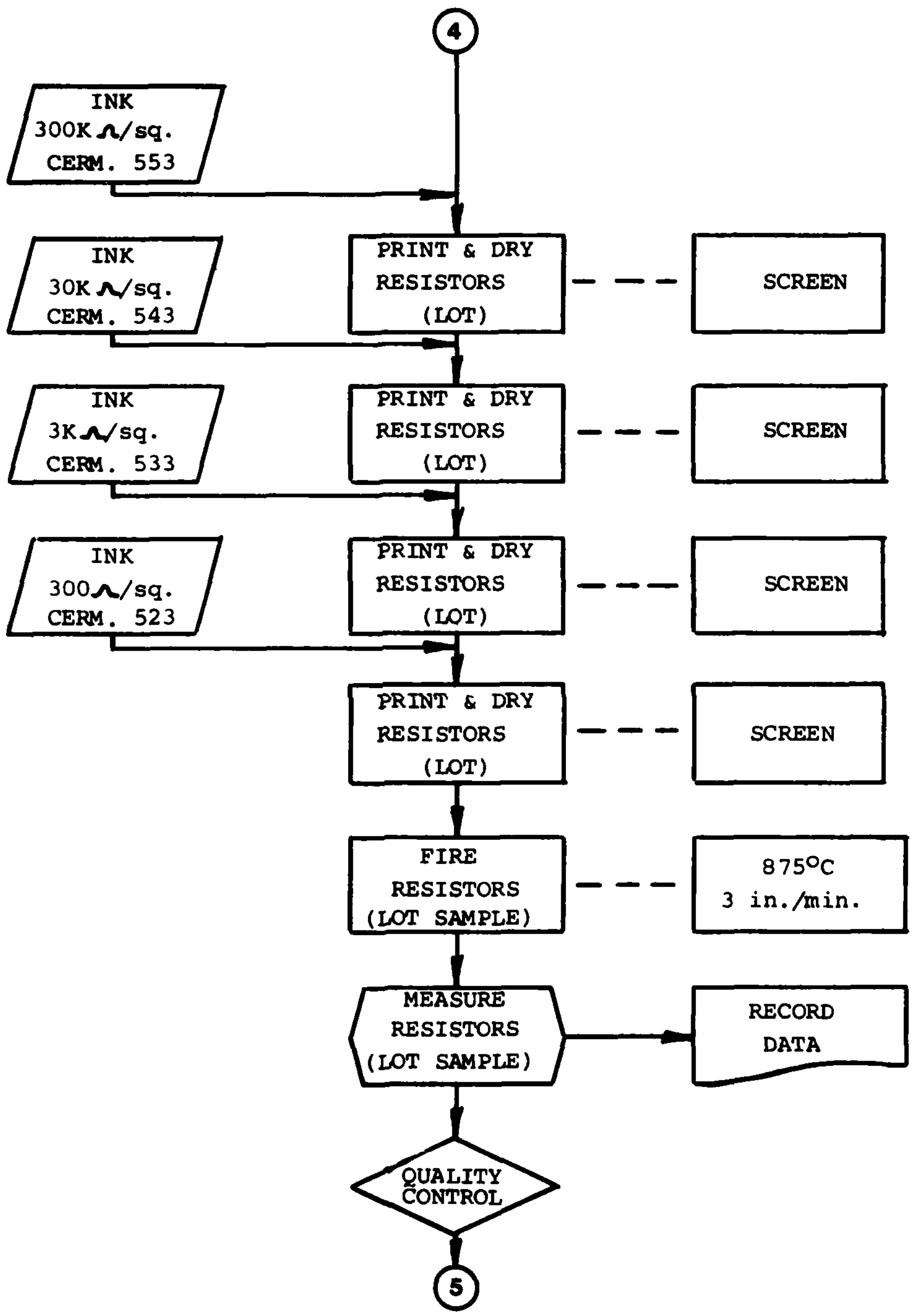
There are no unique requirements in the processing of thick-film substrates other than the eight screens necessary for printing. The yield was commensurate with normal production yields expected in a pilot run production program. However, as it turned out, an unexpected problem did arise with the quality of the gold printing. It was not



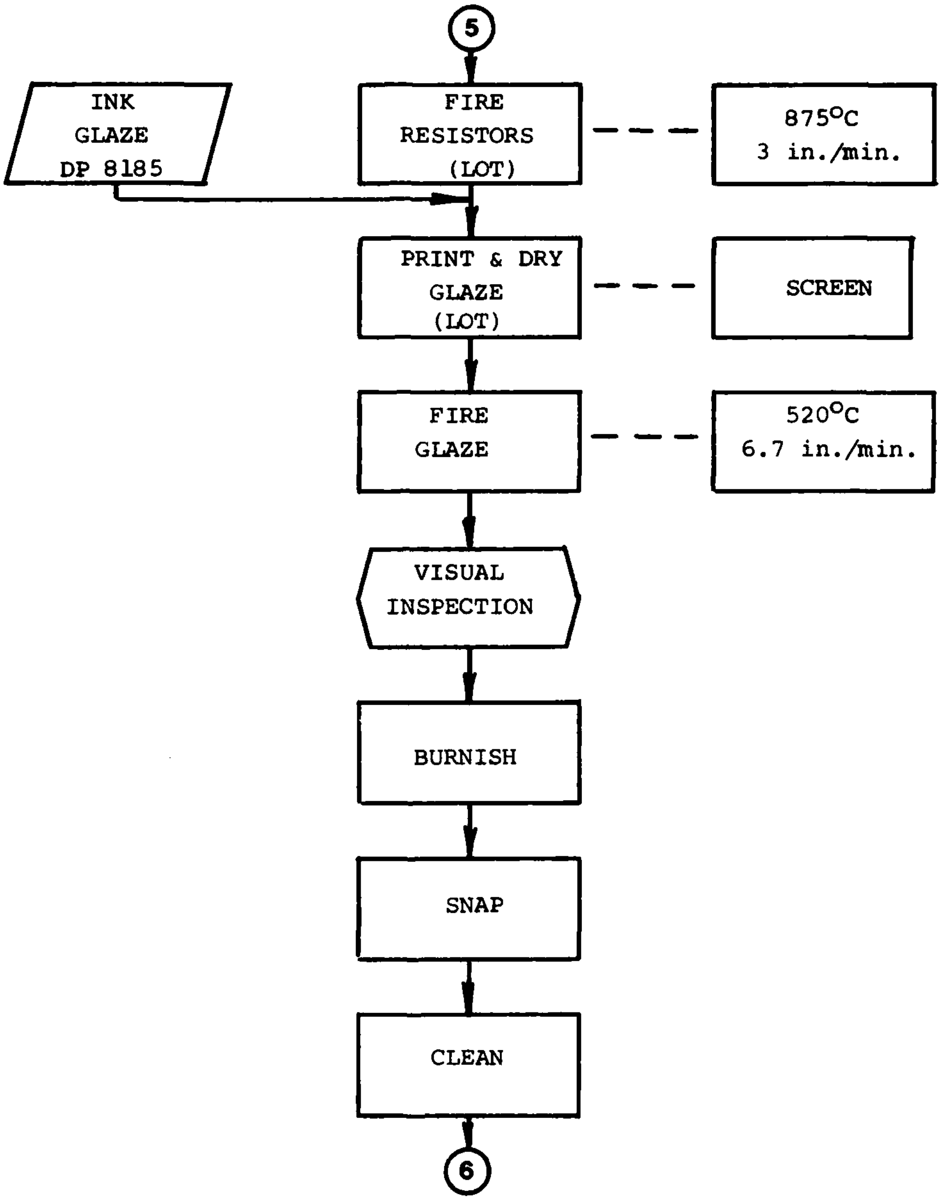
Flow Chart 2. Thick-Film Processing: Printing and Drying Conductors



Flow Chart 3. Thick-Film Processing: Resistor Samples



Flow Chart 4. Thick-Film Processing: Printing and Drying Resistors



Flow Chart 5. Thick-Film Processing: Printing and Drying Glaze

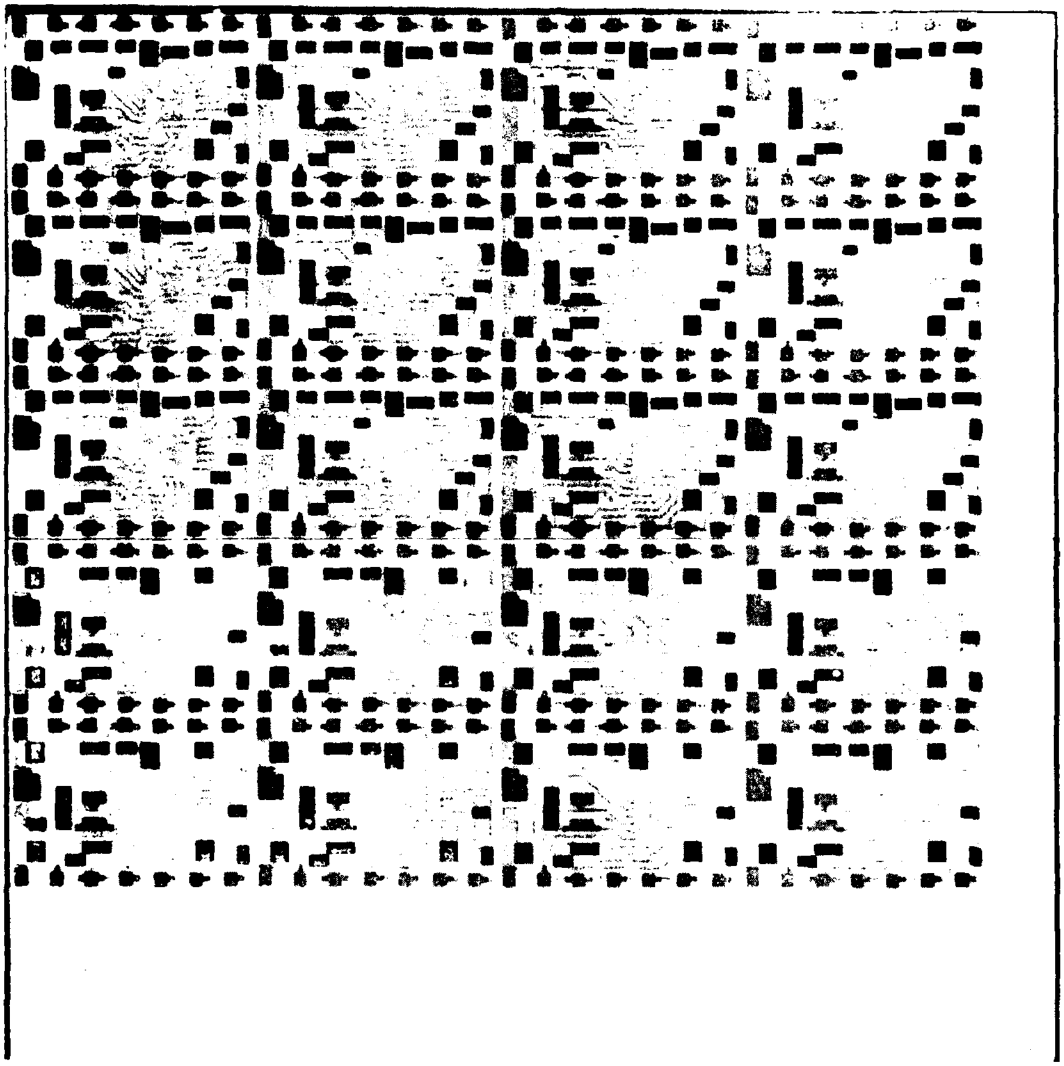


Figure 4. Substrate Fabrication

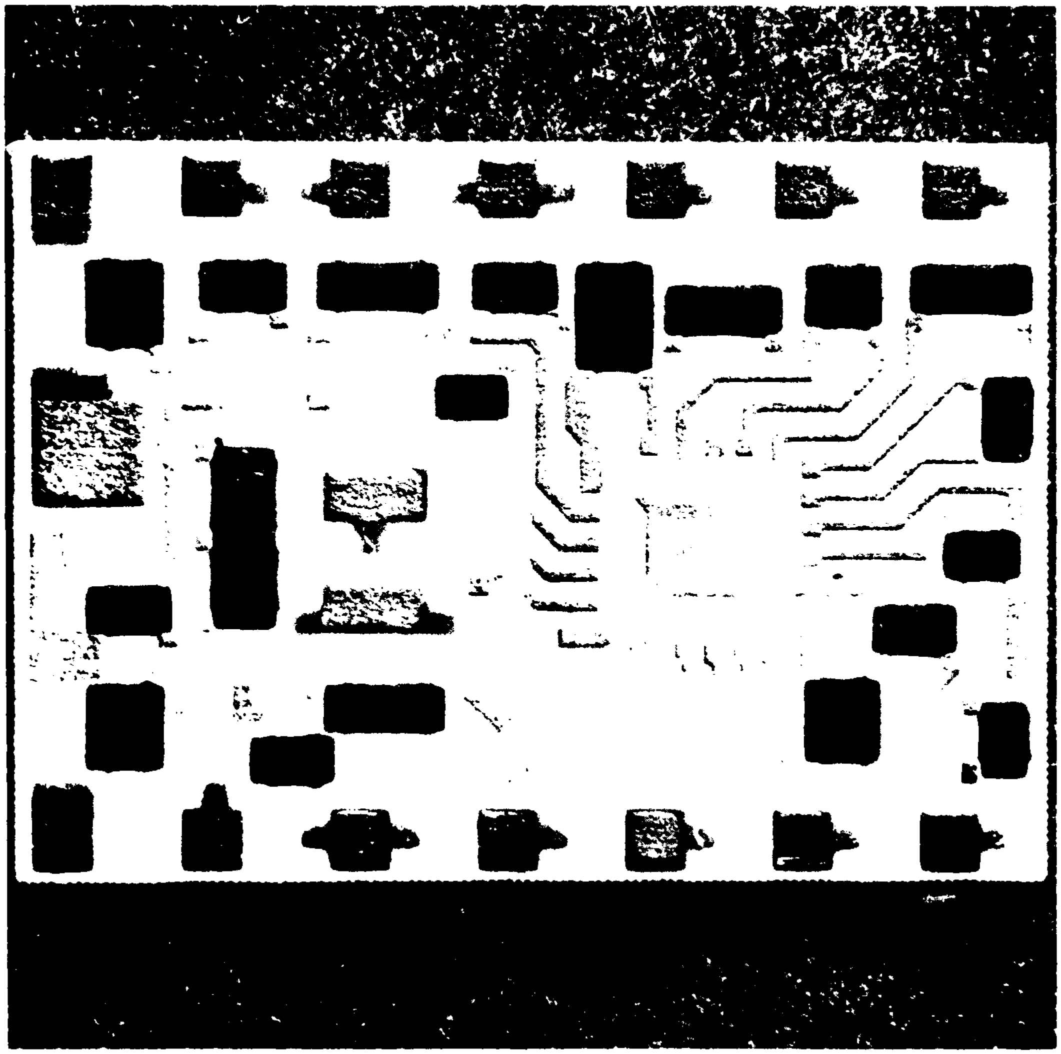


Figure 5. Thick-Film Processing

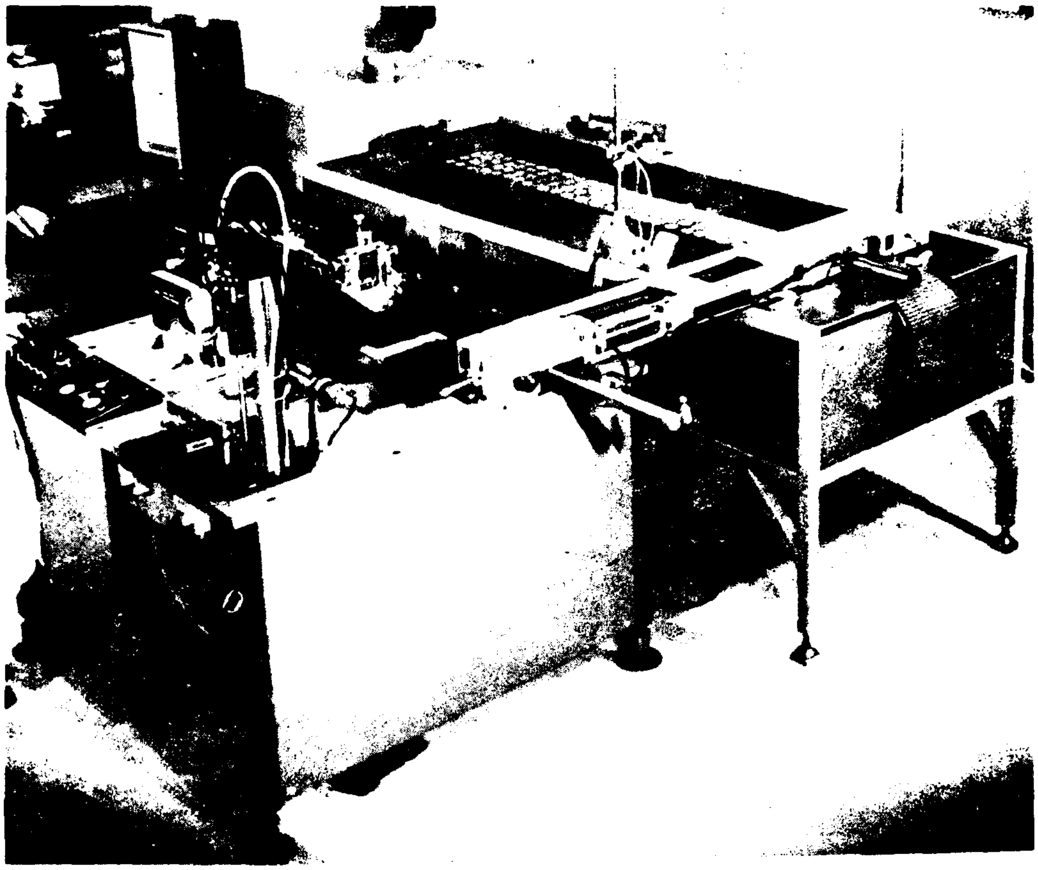


Figure 6. Integrated Printer and Dryer System

discovered until assembly was underway. The problem is discussed under "Substrate Assembly Rework". Increased productivity could be gained if separation of individual units were accomplished after resistor trimming.

Resistor Trimming: These are the substrate fabrication operations associated with resistor trimming (flow chart 6) necessary to laser trim the thick-film substrate resistors at RCA/SSD, Mountaintop, PA. Units are processed individually. A photograph of the thick-film substrate prepared for laser trimming is provided in figure 5.

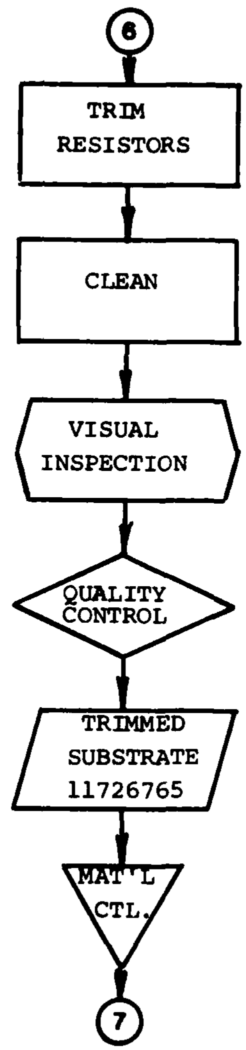
On 23 February 1979, laser trimming of the thick-film substrate resistors began at RCA/SSD. Laser trimming was accomplished in two lots (B1 and B2) to match the two lots of IC chips that would eventually be mounted to the thick-film substrate during hybrid assembly operations.

Three thousand five hundred fourteen thick-film substrates were candidates for laser trimming at RCA/SSD. Eight hundred fifty five units were consumed in setup or rejected during laser trimming. Two hundred of these laser trimming candidates were rejected with R12 resistance values too high for trimming.

The resistor trimming acceptable balance of 2659 units was completed and available at RCA/AS for further processing on 5 March 1979. Two hundred seventy eight units were rejected for visual faults after resistor trimming.

The acceptable balance of 2381 units was available for subsequent hybrid assembly processes on 17 March 1979. With an operational net start quantity of 3514 units and a basic net start quantity of 4300 units, the yield from operations was 67.8 percent, and the yield from net start was 55.4 percent.

There are no unique requirements for laser trimming of the substrate resistors. However, the RCA/SSD, Mountaintop, PA, facilities were only capable of resistor trimming on individual circuits for this program. Increased productivity could readily be gained with a 20 unit step and repeat trimming program. This improvement would not increase the productivity of only laser trimming itself, but the prior and subsequent cleaning operations as well.



Flow Chart 6. Resistor Trimming

Substrate Assembly: These are the hybrid assembly operations associated with substrate assembly (flow charts 7 to 9) necessary to populate trimmed substrate 11726765 with discrete components up to the point where first electrical test and inspection is possible at RCA/AS. Units are processed on an individual basis. A photograph of substrate assembly 11726764 is provided in figure 7. Figures 8 to 10 provide photographs of various substrate assembly equipment.

On 17 March 1979, hybrid assembly operations were started with the initial processing of sublots HD001 through HD006.

Two thousand three hundred eighty one trimmed substrates 11726765 were candidates for substrate assembly at RCA/AS. Three units were withdrawn as engineering samples. Two hundred seventy units were consumed or rejected during the substrate assembly.

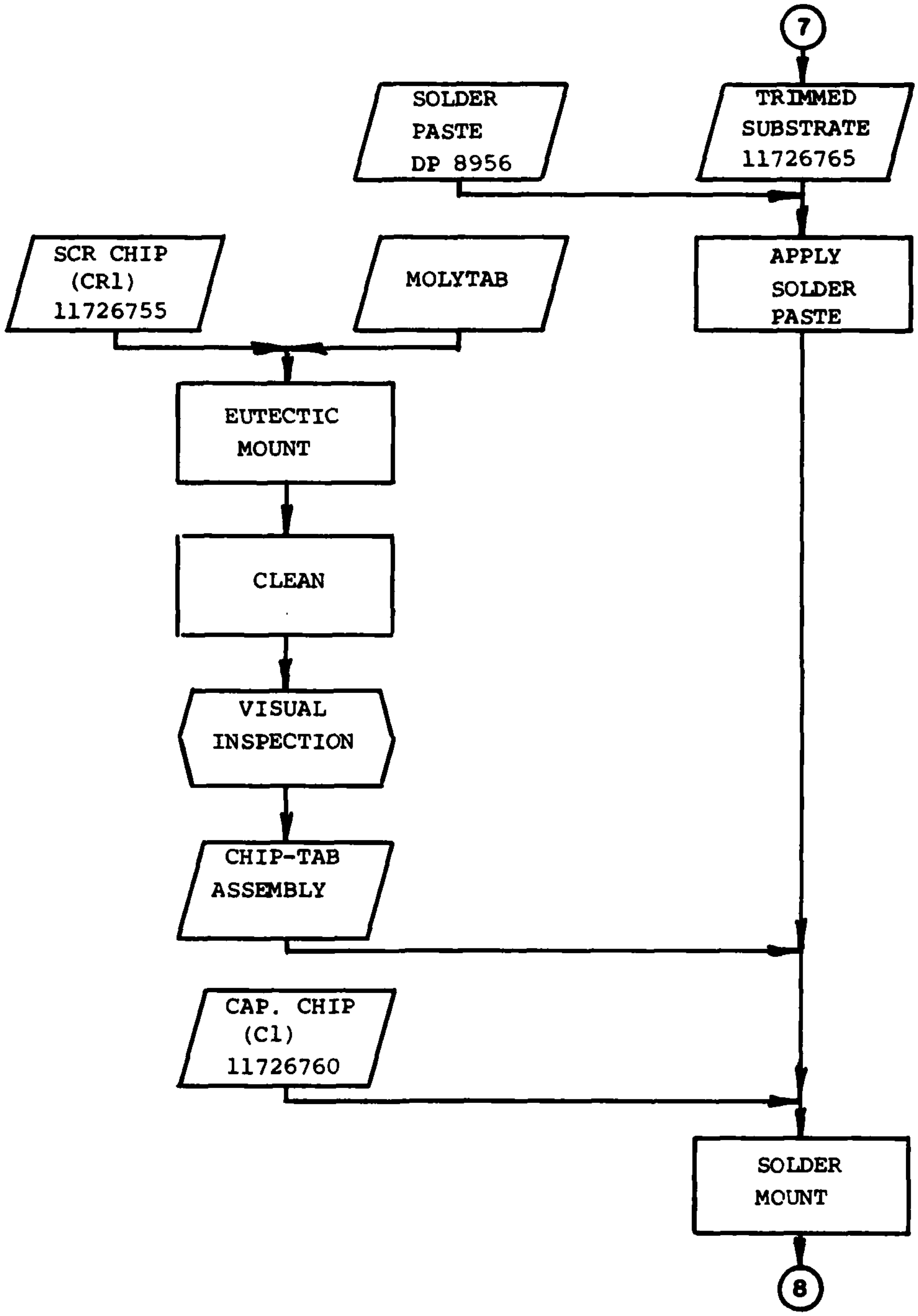
The acceptable balance of 2108 units started to be available for subsequent first electrical test and inspection on 23 May 1979.

With an operational net start quantity of 2378, the yield from operations was 88.6 percent. Since this is the first stage of hybrid assembly, the yield from net start is identical.

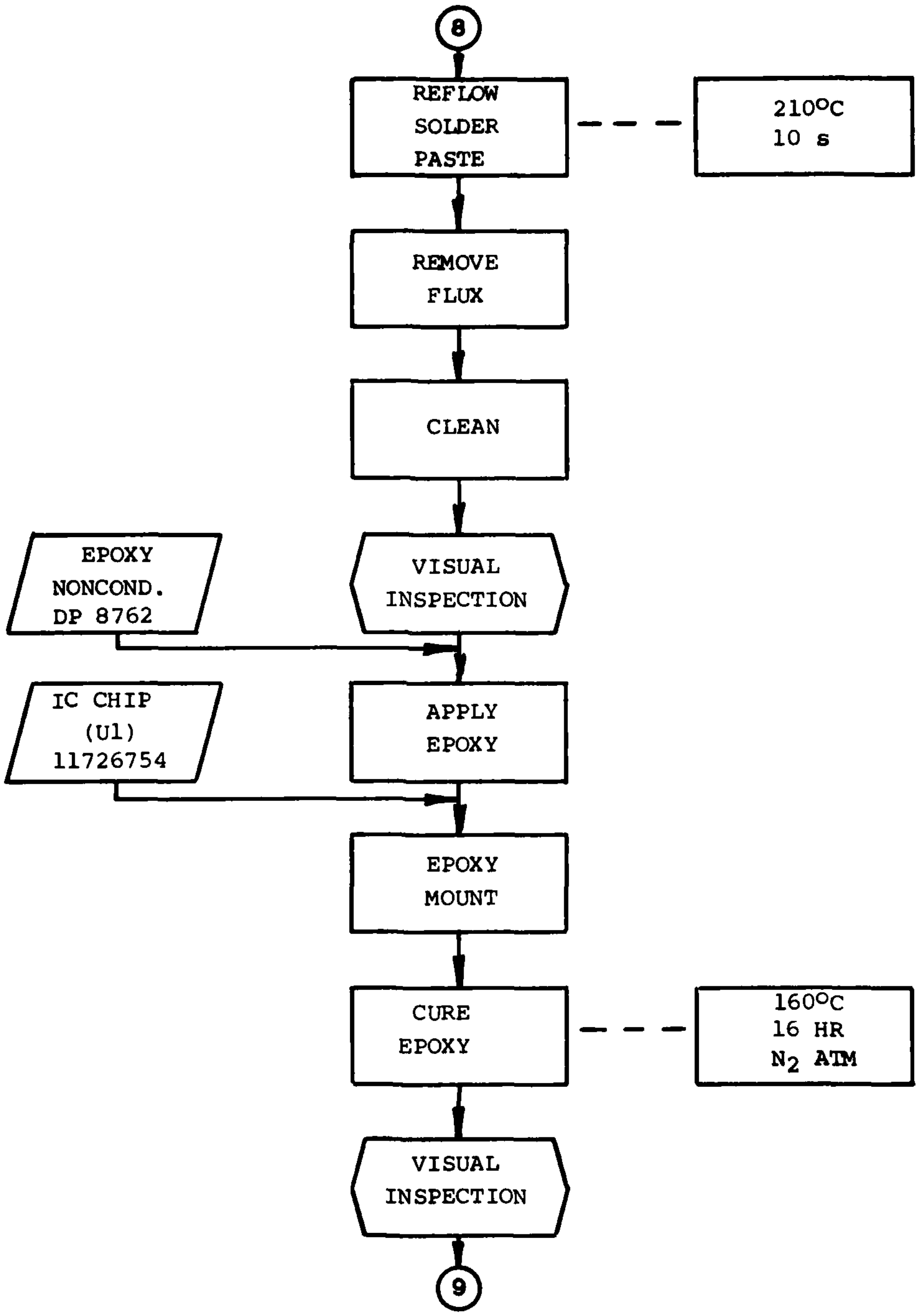
There are no unique requirements for substrate assembly. However, as developed in first electrical test and inspection, unexpected problems were associated with automatic wire bonding. This is discussed under "Substrate Assembly Rework".

First Electrical Test and Inspection: These are the hybrid assembly operations associated with first electrical test and inspection (flow chart 10) necessary to evaluate populated substrate assembly 11726764 at RCA/AS, prior to encapsulation. The unit is fully populated without a lead frame. Units are processed individually. This is the first opportunity for electrical evaluation of the interface circuit and the last opportunity for rework (if required). A photograph of substrate assembly 11726764 is provided in figure 7.

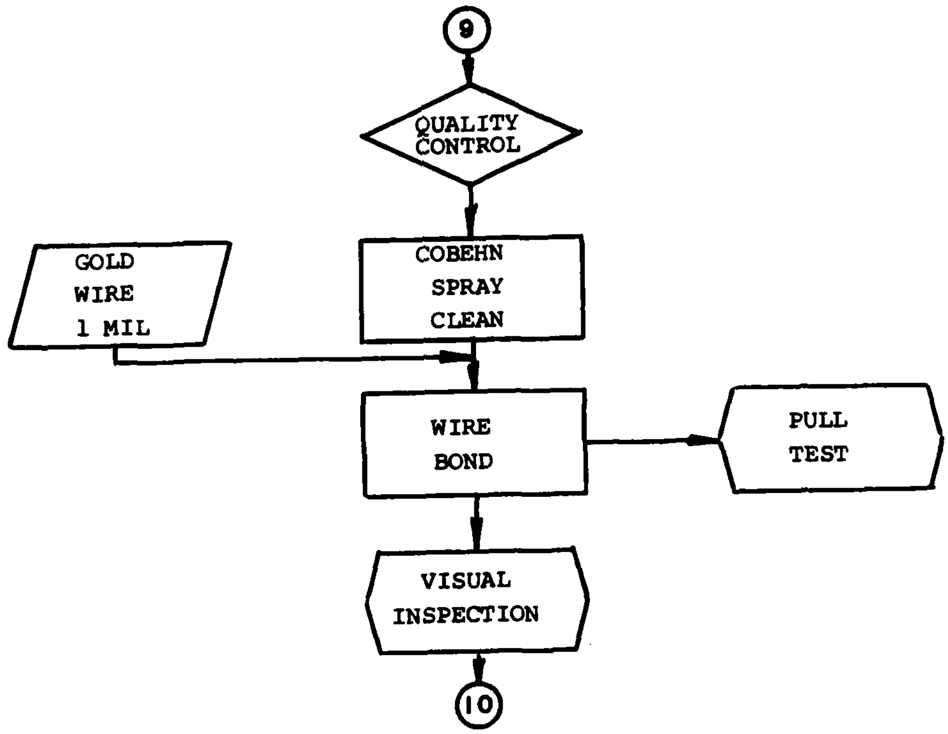
On 23 May 1979, first electrical test and inspection began on substrate assembly sublots HD001 through HD006.



Flow Chart 7. Substrate Assembly: Chip-Tab



Flow Chart 8: Substrate Assembly: IC Chip



Flow Chart 9. Substrate Assembly: Wire Bond

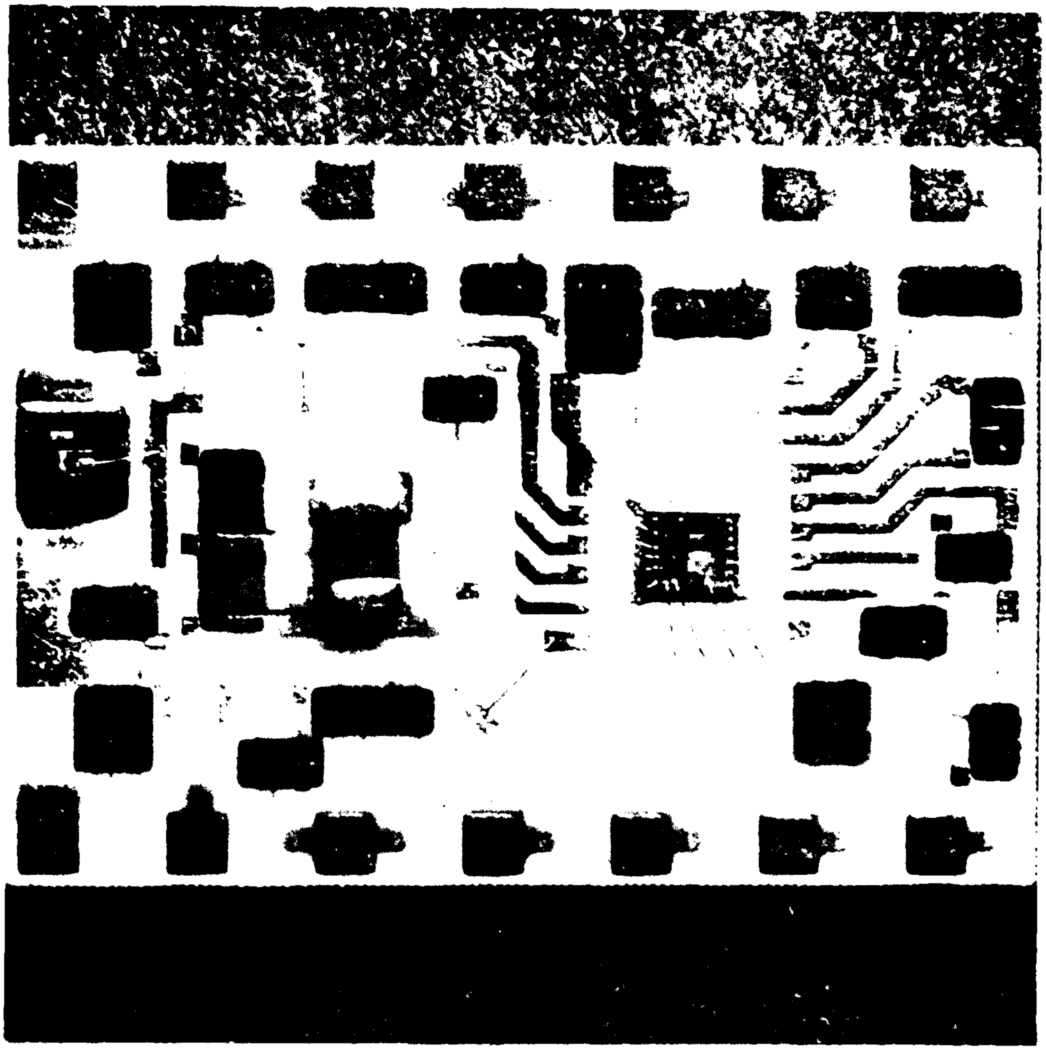


Figure 7. Substrate Assembly

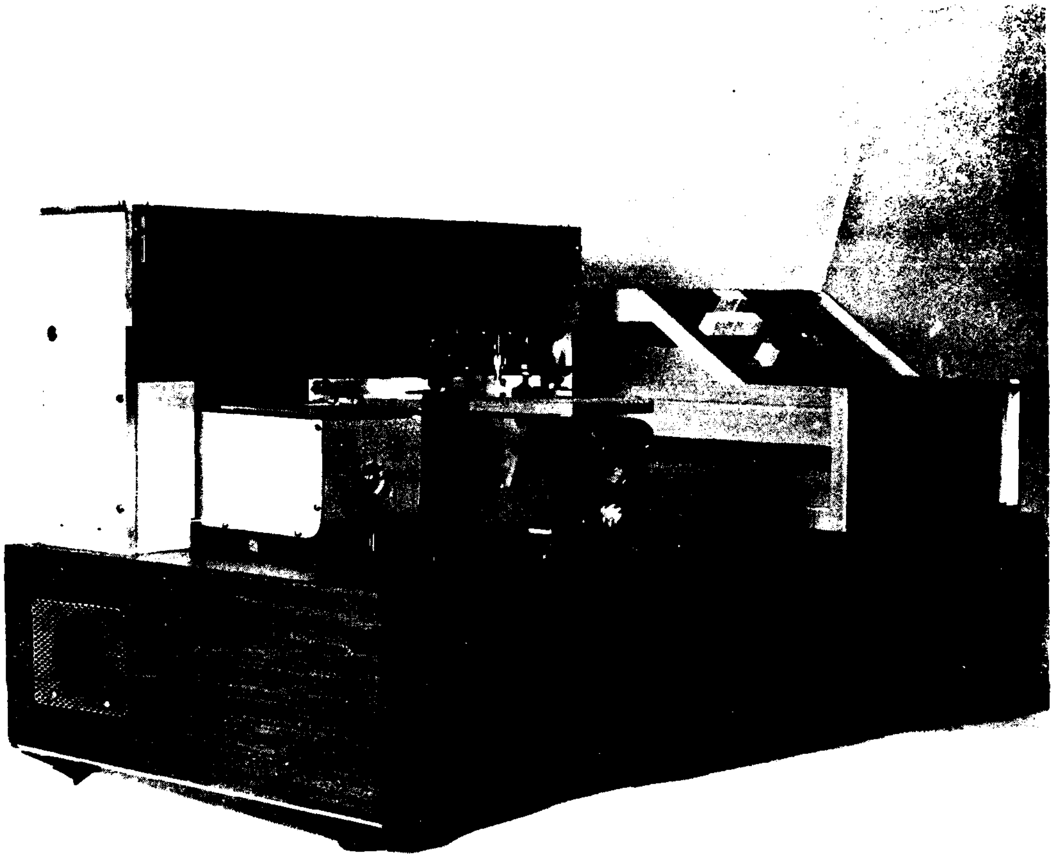


Figure 8. Dixon Robot Chip Assembly

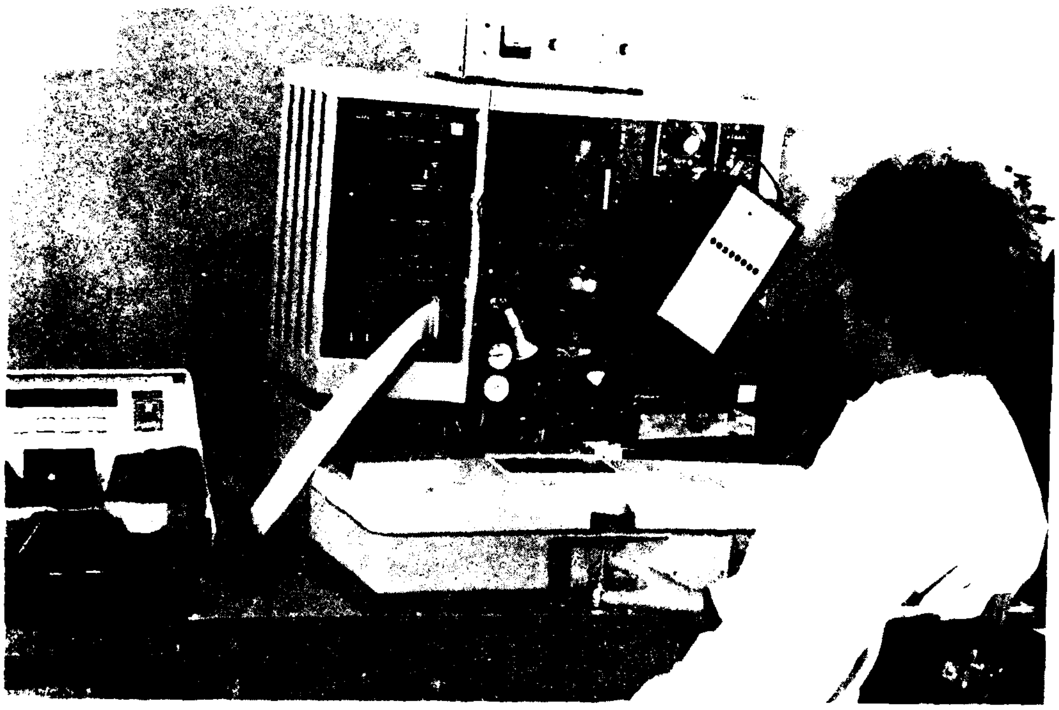


Figure 9. GCA Automatic Wire Bonder

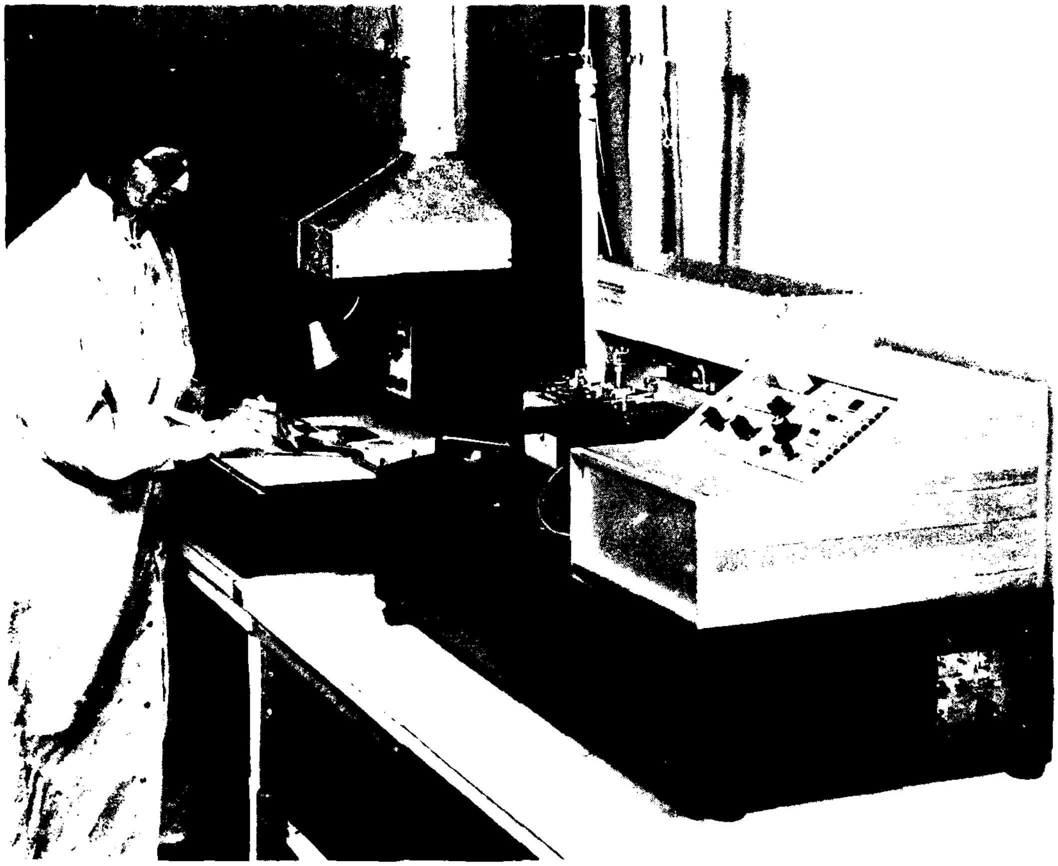
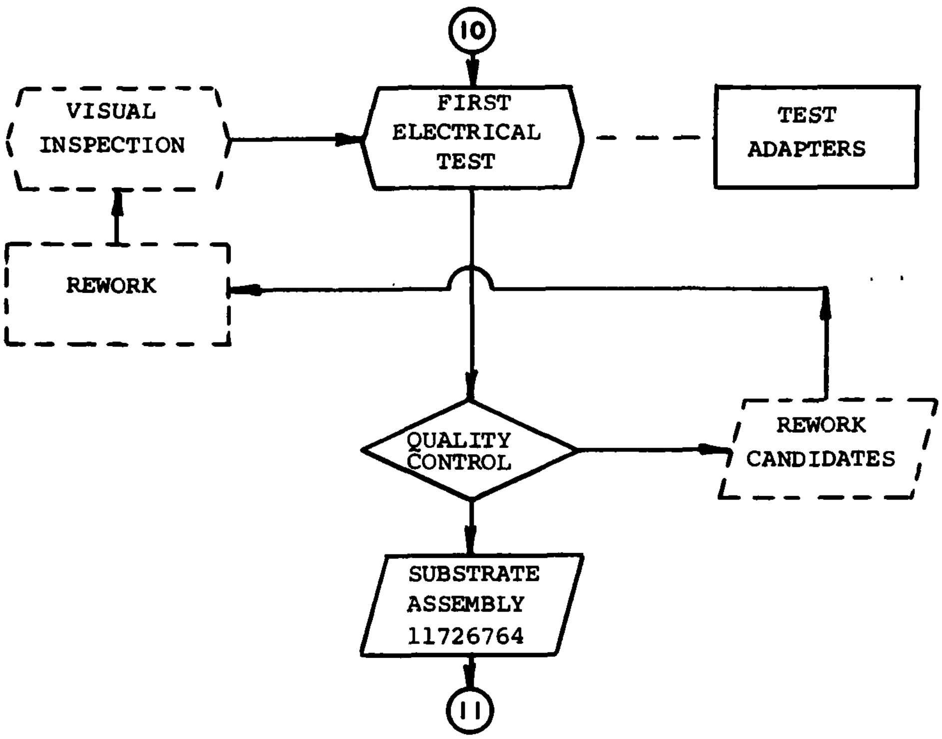


Figure 10. Browne Engineering Rotary Reflow Station



Flow Chart 10: First Electrical Test and Inspection

Two thousand one hundred eight substrate assemblies 11726764 were candidates for first electrical test and inspection at RCA/AS. One thousand one hundred thirty four units were rejected as a result of first electrical test and inspection. Three hundred ninety five of these rejected units became sublot HDR01.

The acceptable balance of 974 units was made available for subsequent encapsulation on 23 May 1979.

With an operational net start quantity of 2108 units and a basic net start quantity of 2378 units, the yield from operations was 46.2 percent, and the yield from net start was 41.0 percent without benefit of assembly rework quantities. With the addition of assembly rework quantities, the yield from net start increased to 45.8 percent.

There are no unique requirements for first electrical test and inspection other than the special test equipment itself, the probe card adapter, and in-line test set BTA-2-2199.

Substrate Assembly Rework: During substrate assembly, problems arose in the wire bonding. In an effort to resolve the poor wire bonds, the bonding pads were manually eraser burnished. Inadvertently, in the burnishing, the chip surfaces were also scratched. This additional problem was not discovered until first electrical test and inspection of the burnished units. All the electrical test rejections up to that time were evaluated, and sublot HDR01 was formed from the unsegregated rejections of sublots HD001 through HD004.

After evaluation of all the conditions that could have contributed to the poor quality wire bonds, it was resolved that the basic problem had been poor quality thick-film gold pads from the substrate fabrication. This problem had not been anticipated and is abnormal in production.

On 6 June 1979, 395 rework candidates were available for chip replacement. Of these rework candidates, 185 units were reworked and reentered into production at first electrical test and inspection. It was directed by HDL that no additional rework was to be expended on the balance of 210 candidates for rework in sublot HDR01 or on any other rejected units that might be candidates for rework. Seventy one units in sublot HDR01 were rejected.

The acceptable balance of 114 units was made available for subsequent encapsulation on 3 July 1979.

With an operational net start quantity of 185 units, the yield from operations was 61.6 percent.

Substrate assembly rework is included normally during the early stages of production. This effort is deemed cost effective until experience is gained and IC chip yield surpasses 85 percent. Discontinuation of the substrate assembly rework program can be anticipated as being cost effective at higher yield levels.

Encapsulation: These are the hybrid assembly operations associated with encapsulation (flow chart 11) necessary to protect chips, crossovers, and bond wires from damage during transfer molding. Encapsulation was performed at RCA/AS, and units are processed individually. For a summary of this operation, refer to section 2.2.1. A photograph of the encapsulated substrate assembly is provided in figure 11.

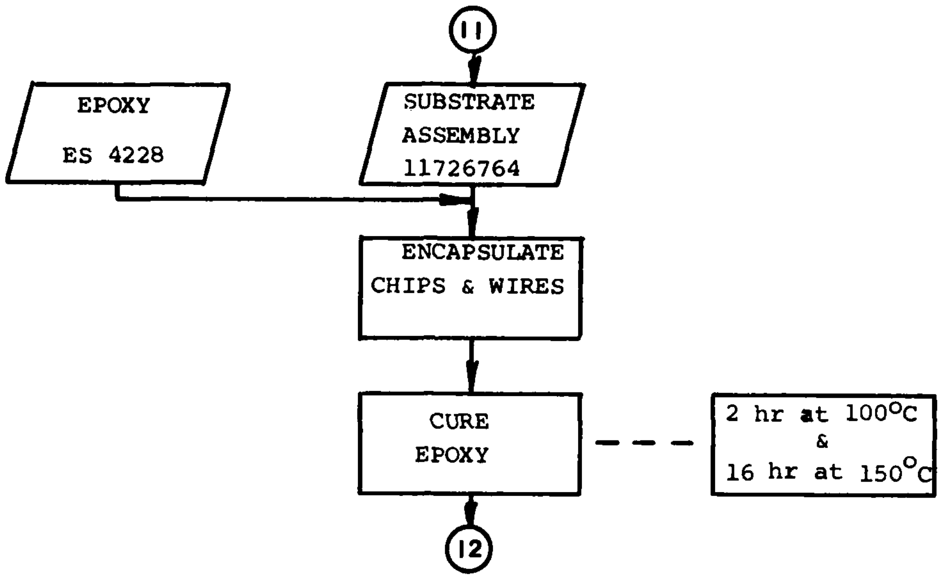
On 23 May 1979, encapsulation began for sublots HD001 through HD006 and HDR01.

One thousand eighty eight units were candidates for encapsulation. Since this is a relatively simple process, there were no rejections.

The acceptable balance of 1088 units started to be available for lead frame assembly on 1 June 1979.

Without rejections, the yield from operations was 100 percent. With a basic net start quantity of 2378 units, the yield from net start was 45.8 percent including reworking.

There are no unique requirements for encapsulation. However, as mentioned in section 2.3.2, for production, the capacitor should also be encapsulated for additional strength and protection.



Flow Chart 11. Encapsulation

Figure 11. Encapsulation

Lead Frame Assembly: These are the hybrid assembly operations associated with lead from assembly (flow chart 12) necessary to attach the encapsulated substrate to a lead frame. Lead frame assembly was accomplished at RCA/AS in multiples of six units. Up to this point, hybrids have been assembled individually. From this point through transfer molding, process operations are performed in multiples of six. A photograph of the assembly, premold 11726763, is provided in figure 12.

On 1 June 1979, lead frame assembly began for sublots HD001 through HD006 and HDR01.

One thousand eighty eight units were candidates for lead frame assembly at RCA/AS. Twenty four units were consumed or rejected during the lead frame assembly.

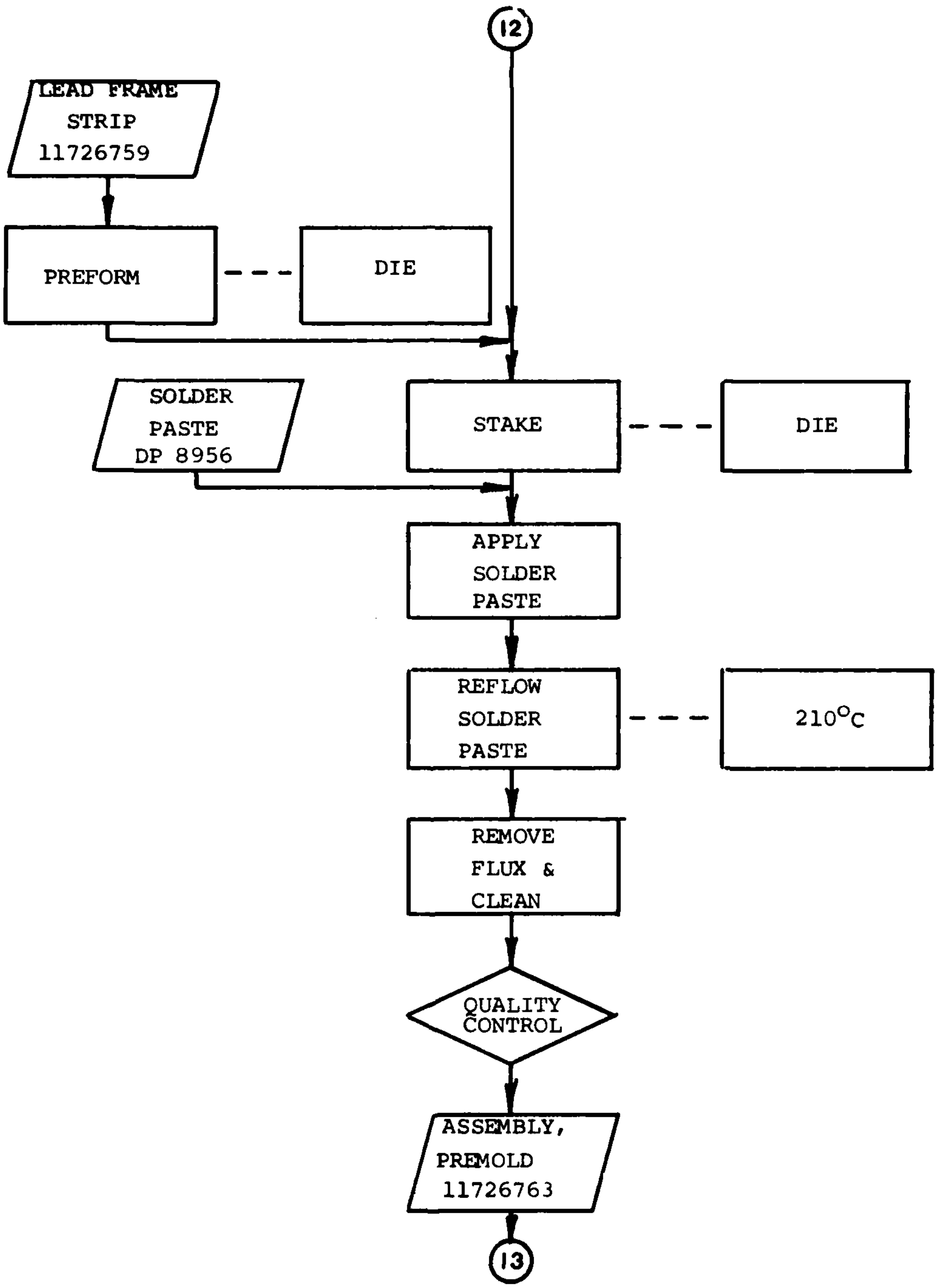
The acceptable balance of 1064 units started to be available for subsequent transfer molding at RCA/SSD on 2 July 1979.

With an operational net start quantity of 1088 units and a basic net start quantity of 2378 units, the yield from operations was 97.8 percent, and the yield from net start was 44.7 percent.

There are a number of unique requirements for the lead frame assembly. Two special dies are required - a lead frame preform die to offset the 14 leads (of each unit) to accept the substrate assembly and a lead frame staking die to stake the substrate assemblies in place in the six unit lead frame for soldering. In addition, special hot plate reflow soldering was instituted to improve quality. These processes are delineated in special process instructions.

Transfer Molding: These are the hybrid assembly operations associated with transfer molding (flow chart 13) necessary to encase the interface circuit in protective plastic. Transfer molding was accomplished at RCA/SSD, Somerville, NJ in multiples of six units. A photograph of the molded assembly, 11726762, is provided in figure 13.

On 2 July 1979, ML-1, consisting of the 537 acceptable units from sublots HD001 through HD004, was shipped to RCA/SSD for transfer molding. On 16 July 1979, ML-2, consisting of 527 acceptable units from sublots HD005, HD006, and HDR01, was shipped for transfer molding.



Flow Chart 12. Lead Frame Assembly

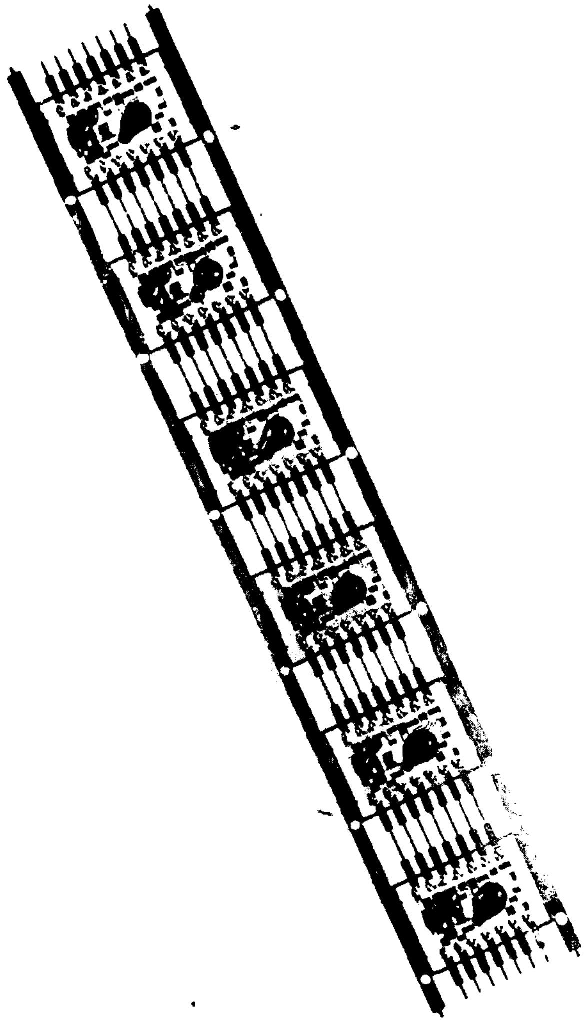
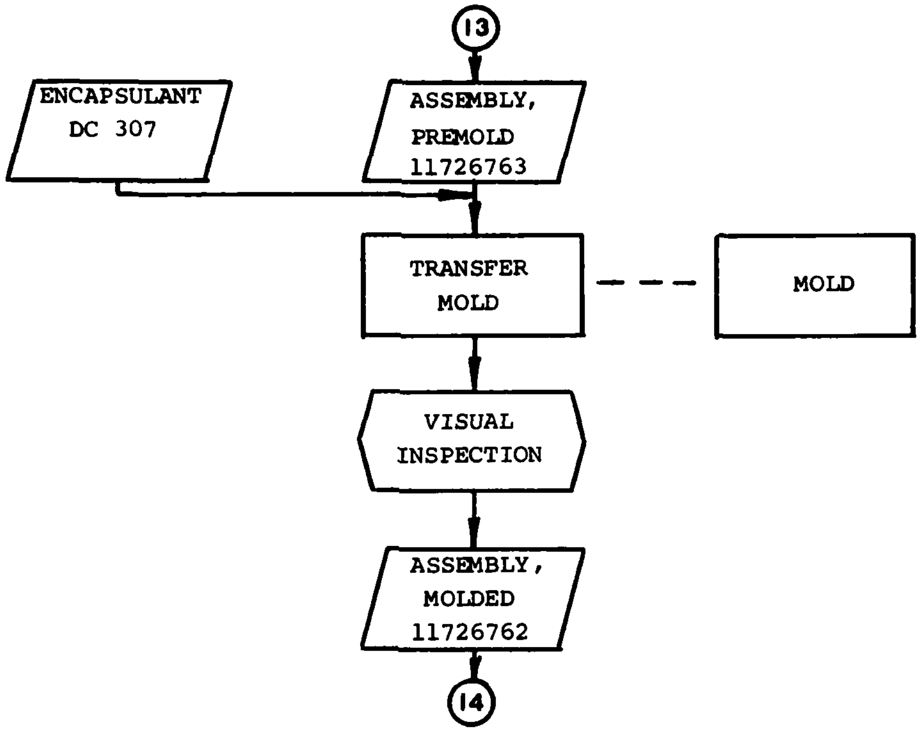


Figure 12. Lead Frame Assembly



Flow Chart 13. Transfer Molding

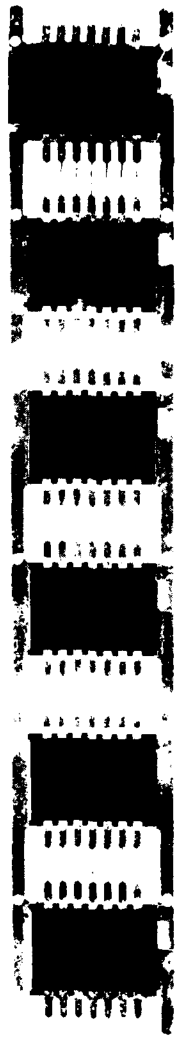


Figure 13. Transfer Molding

One thousand sixty-four units were candidates for transfer molding at RCA/SSD. Sixty units were rejected as a result of mold voids in the interface circuit, 59 of which were in ML-1 corrected in ML-2 to one mold void reject. Mold rejections are discussed in the next section.

The acceptable balance of 1004 units started to be available for subsequent separation and marking operations at RCA/AS on 19 July 1979.

With an operational net start quantity of 1064 units and a basic net start quantity of 2378 units, the yield from operations was 94.4 percent, and the yield from net start was 42.2 percent.

All sublots were segregated from each other in each mold lot and identified as such during the transfer molding operations. Two material colors were used in transfer molding. ML-1 was completed with a black molding material. ML-2 was started with the same material. However, insufficient black material was available for lot completion. A gray material was available, so in the interest of schedule expediency and with the prior approval of HDL, ML-2 was completed with the gray material.

There are no unique requirements for tranfer molding other than the six cavity transfer mold itself. Although this application of transfer molding is original, the process itself is well known. Techniques for this application can be readily fine tuned over time for improved productivity. Adjustments in the tooling are needed as discussed under special tooling, and further experience must be gained with the molding material itself. It was agreed that microcracks, hairline cracks at the surface of the molded product which did not expose the contents, were not cause for rejection. Mold voids, those surface defects that expose the contents of the molded product, are cause for rejection.

<u>Mold Reject Reevaluation</u>: In an effort to improve the quality and, therefore, the yield in the transfer molding operations performed at RCA/SSD, Somerville, NJ, it was found to be advantageous to provide additional mold relief at certain mold cavities of the six unit mold. This was accomplished by snipping a portion of the lead frame longitudinal carrier. This is clearly shown in the photograph of the assembly, molded 11726762, figure 13. Due to a lack of good communication during our program management changeover, it had been falsely assumed that each unit associated with this mold relief was designated by RCA/SSD as

a mold reject. Upon separation from the lead frame carrier, these so-called SSD mold rejects were set aside from the two mold lots in an unsegregated container labeled SSD mold rejects. This error was later recognized, and the SSD mold rejects were reevaluated. Sublot HD007 was formed from these unsegregated units. Of the 207 units so designated, 144 were reclassified as fully acceptable units after electrical test and visual inspection. These 144 units were reentered into production. Upon final electrical test, of these units, 134 units passed and were submitted to HDL on 30 October, 1979 as shipping lot 7941. Interestingly, of all the units produced, these units were the only units subjected to electrical test just prior to and immediately following marking. Ten units were lost during these operations. The suspected cause for the 7 percent loss during the marking operation is the one part epoxy ink curing requirement of 150°C. Future consideration should be made to reduce the curing temperature by the use of a two part epoxy ink in place of the present ink specified.

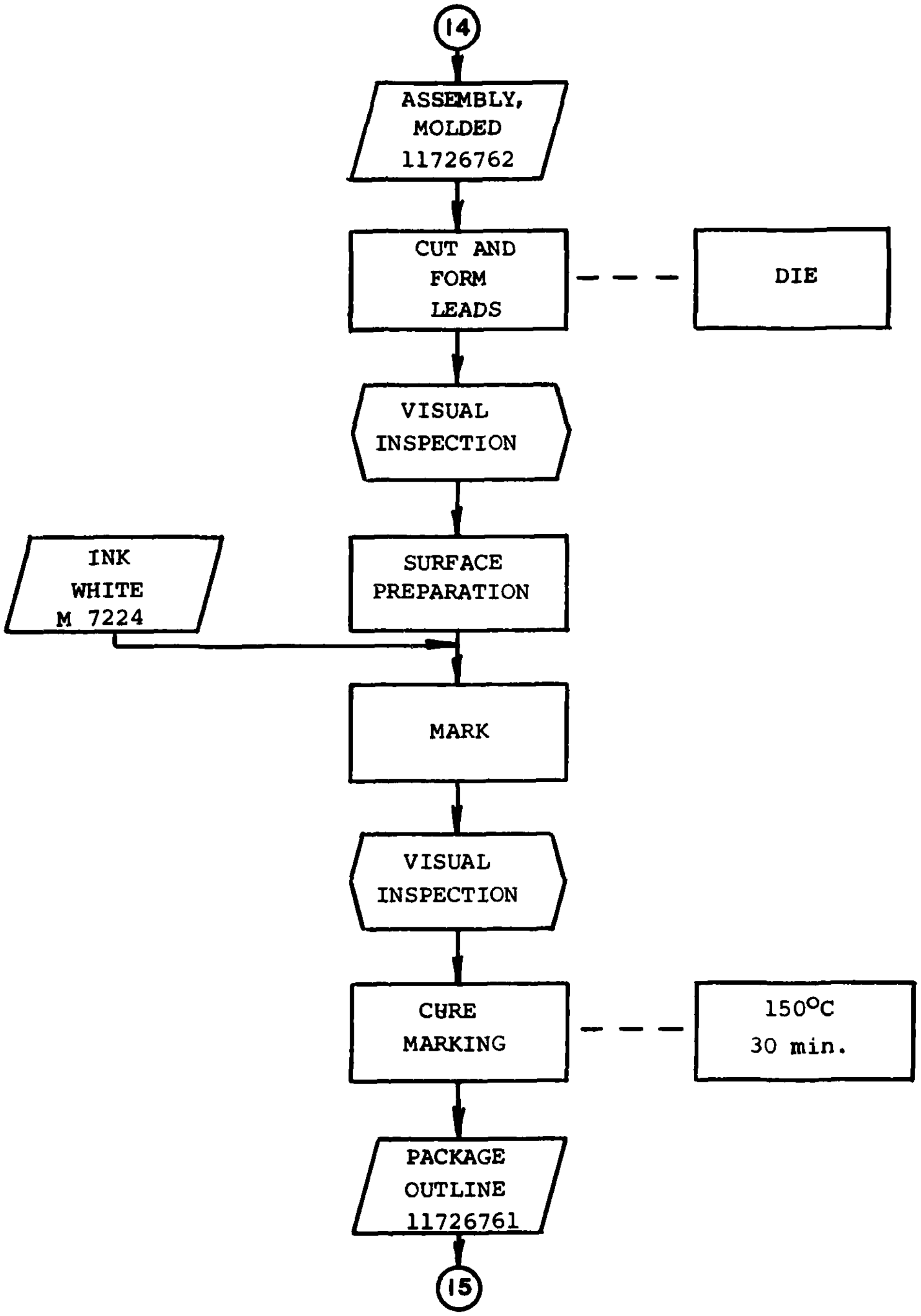
Marking: Flow chart 14 shows the hybrid assembly operations necessary to separate the individual units from the molded assembly 11726762, while cutting and forming leads, and to mark them per package outline 11726761. These operations were accomplished at RCA/AS and processed individually. A photograph of the product before these operations is provide in figure 13 and after these operations in figure 14.

On 19 July 1979, ML-1 began the separation operations; on 8 August 1979, ML-2 began the separation operations; and on 10 October 1979, SSD mold reject reevaluation sublot HD007 began marking operations.

One thousand four units were candidates for marking at RCA/AS. Eight units were consumed or rejected during separation and marking.

The acceptable balance of 996 units started to become available for subsequent final electrical test and inspection on 24 July 1979.

With an operational net start quantity of 1004 units and a basic net start quantity of 2378 units, the yield from operations was 99.2 percent, and the yield from net start was 41.9 percent.



Flow Chart 14. Lead cutting and forming and unit marking.

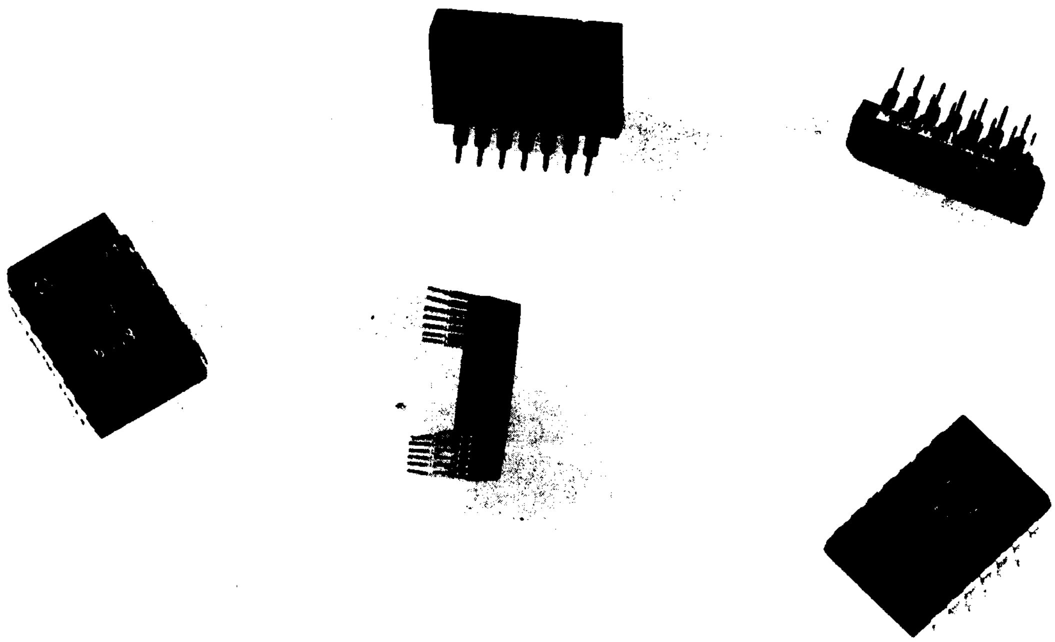


Figure 14. Completed Units

Date codes and shipping lot numbers (7928, 7932, 7932R, and 7941) are synonymous. These numbers consist of the year of manufacture (79) plus the production week of marking (28, 32, and 41). The alphabetical suffix (R) indicates the rework lot.

There are a number of unique requirements for these operations. A lead frame cut and forming die is required to separate the individual units from the six unit assembly, molded 11726762, and to form the 14 leads. Surface preparation is required on the molded product for the acceptance of the marking ink. This process is fully delineated in special process instruction SPI-2039. As discussed in the previous section, consideration should be given to a change in marking material.

Final Electrical Test and Inspection: These are the hybrid assembly operations associated with final electrical test and inspection of the product (flow chart 15) necessary to evaluate the product for acceptance. This evaluation was accomplished at RCA/AS and processed individually. A photograph of completed interface circuit SCD 11726909 is provided in figure 14.

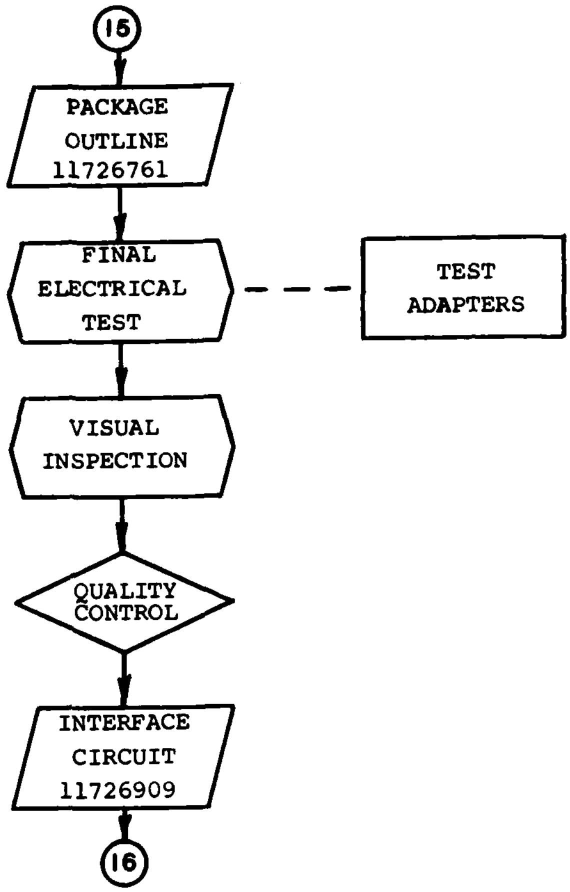
On 24 July 1979, interface circuits began the final electrical test and inspection processes with ML-1, shipping lot 7928. ML-2 shipping lots 7932 and 7932R followed on 10 August 1979, and shipping lot 7941 started on 10 October 1979.

Nine hundred ninety six units were candidates for final electrical test and inspection at RCA/AS. Two hundred thirty two units were rejected. Sixty four of these rejected units were red leads (although electrically acceptable, they were known mechanical rejections internally).

The acceptable balance of 764 units started to be packaged for shipment in the comparison sample on 12 September 1979.

With an operational net start quantity of 996 units and a basic net start quantity of 2378, the yield from operations was 76.7 percent, and the yield from net start was 32.1 percent.

Although the records indicate that 764 units were acceptably completed, 775 units were actually shipped as acceptable units. The discrepancy of 11 units is unaccounted for.



Flow Chart 15. Final Electrical Test and Inspection

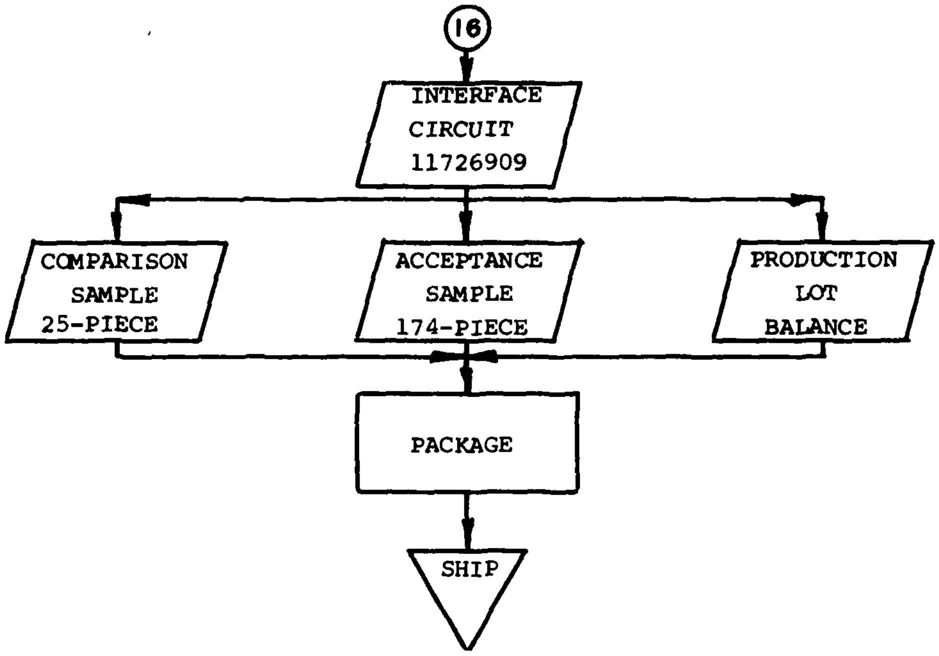
There are no unique requirements for in-line production test (versus acceptance test) of interface circuit SCD 11726909 other than the special test equipment in-line test set BTA-2-2199.

Packaging and Shipping: Table VII lists the quantity of units packaged and shipped to HDL.

TABLE VII - PACKAGING AND SHIPPING DATA - PHASE IV

Date	Quantity	Lot	Comments
8/15/79	25	7932	Subgroup B2 - Mechanical Shock S/N 51-75
8/15/79	25	7932	Subgroup C1 - Gunfire S/N 126-150
9/12/79	12	7928	Comparison sample
9/12/79	13	7932	Comparison sample
9/17/79	101	-	Electrical Rejects with Data
10/30/79	125	7932	Acceptance Test Sample S/N 1-125
10/30/79	8	7932	Acceptance Test Sample S/N 151-158
10/30/79	16	7932	Acceptance Test Sample S/N R1-R16
10/30/79	289	7928	Pilot Production Run - Lot Balance
10/30/79	92	7932	Pilot Production Run - Lot Balance
10/30/79	77	7932R	Pilot Production Run - Lot Balance
10/30/79	134	7941	Pilot Production Run - Lot Balance

One unit from the comparison sample was returned informally to RCA/AS as defective; refer to section 2.4.2. Retest at RCA confirmed the failure, and the unit was returned to HDL. Flow Chart 16 shows the packaging and shipping process.



Flow Chart 16. Packaging and Shipping

2.4.2 Production Quantity and Yields

Copies of all nine phase IV travelers are provided in the manufacturing notebook.

The actual phase IV travelers have been consolidated into the four shipping lot travelers provided in appendix B as follows:

Shipping Lot (Date Code)	Substrate Assembly Sublot	Trimming Lot
7928	HD001 through HD004	B2
7932	HD005 and HD006	B1
7932R	HDR01	B2
7941	HD007	B1 and B2

A consolidation of all travelers for the entire phase IV is provided in table VIII. Although there are mathematical deficiencies in this table as a result of record keeping deficiencies in the program, this table is the basis for all data supplied in the text.

The actual program quantity and yield date, table IX, is a consolidation of the data from table VIII into the various functional activity production process operations as discussed in section 2.4.1.

Appreciable time and effort have been expended in an attempt to reconstruct actual program records. For future requirements, it is highly recommended that greater stress be applied to keeping records because accurate yield is of paramount importance for evaluation. In addition, setup requirements concerning consumption of products demand greater attention.

2.4.3 Testing/Test Results

Seven hundred seventy-five units were determined to be acceptable for delivery after test and evaluation at RCA/AS. Acceptance testing of samples of the production lot was performed in accordance with the requirements summarized by table X.

TABLE VIII - PILOT PRODUCTION RUN
CONSOLIDATED PROGRAM TRAVELER - PHASE IV

Production Operations	Quantity			
	Start	Sample	Reject	Accept
Clean Substrate	4420	0	0	4420
Print/Dry/Fire Backside	4420	0	0	4420
Print/Dry/Fire Conductors	4420	40	0	4380
Print/Dry/Fire Resistors	4380	80	0	4300
Print/Dry/Fire Glaze	4300	0	0	4300
Burnish	4300	0	0	4300
Snap and Clean	4300	0	786	3514
Trim Resistors	3514	0	855	2659
100% Visual Inspection	2659	0	278	2381
Quality Control Inspection	2381	0	0	2381
Apply Solder Paste	2381	0	0	2381
Mount Cap. SCR Assembly	2381	0	15	2366
Reflow Solder	2366	0	0	2366
Remove Flux	2366	0	0	2366
Freon Clean	2366	0	0	2366
Epoxy Mount IC/Cure	2366	0	5	2361
100% Visual Inspection	2361	0	173	2188
Quality Control Inspection	2188	3	10	2175
Cobehn Spray Clean	2175	0	0	2175
Wire Bond	2175	0	67	2108
100% Visual Inspection	2108	0	0	2108
100% Electrical Test	2108	0	943	1165
Quality Control Inspection	1165	0	77	1088
Epoxy Coat Wires/Cure	1088	0	0	1088
Prepare Lead Frame Strip	1088	0	0	1088
Mount Substrate to Lead Frame	1088	0	2	1086
Apply Solder Paste	1086	0	2	1084
Reflow Solder	1084	0	14	1070
Remove Flux	1070	0	0	1070
Quality Control Inspection	1070	0	7	1063
Pack for Shipment	1064	0	0	1064
Transfer Mold	1064	0	60	1004
Cut and Form Leads	1004	0	1	1003
Mark and Cure	1003	0	7	996
Final Electrical Test	996	0	168	828
Quality Control Inspection	828	0	64	764
Comparison Sample	25	-	-	25
Acceptance Sample	174	-	16	158
Pilot Lot Balance	592	-	-	592
Pack for Delivery	892	-	117	775
Total Shipment	892	-	117	775

TABLE IX - PILOT PRODUCTION RUN QUANTITY AND YIELD DATA - PHASE IV

Production Process Operations	Quantity					Yield (%) from	
	Start	Setup Sample	Net Start	Reject	Accept	Oper.	Net Start
Substrate Fabrication							
Thick-Film Processing	4420	120	4300	786	3514	81.7	81.7
Resistor Trimming	3514	0	3514	1133	2381	67.8	55.4
Hybrid Assembly							
Substrate Assembly	2381	3	2378	270	2108	88.6	88.6
1st Electrical Test	2108	0	2108	1134	974	46.2	41.0
Assembly Rework	185	0	185	71	114	61.6	04.8
Encapsulation	1088	0	1088	0	1088	100.%	45.8
Lead Frame Assembly	1088	0	1088	24	1064	97.8	44.7
Transfer Molding	1064	0	1064	60	1004	94.4	42.2
Marking	1004	0	1004	8	996	99.2	41.9
Final Electrical Test	996	0	996	232	764	76.7	32.1
Package and Ship	-	-	-	117	775	101.4	32.6

Comparison Sample: The phase IV comparison sample, in conformance with contract paragraph F.9.2, was submitted to HDL on 12 September 1979. The 25 unit comparison sample was drawn randomly from two lots. Twelve units were drawn from lot 7928, and 13 units were drawn from lot 7932. One unit was returned as defective on 18 October 1979. Upon retest at RCA/AS, it was confirmed that this unit did not meet the requirements of V2B, V1B, V1BD, or IR42.

Acceptance Sample: The phase IV acceptance sample balance, in conformance with contract paragraph F.9.3 and table VII, was submitted to HDL on 30 October 1979. The 174 unit acceptance sample was drawn randomly from lot 7932 and serialized in two series. Serial numbers 1 through 158 were consigned to electrical test and evaluation. Serial numbers R1 through R16 (drawn from electrical rejections) were consigned to mechanical test and evaluation. Twenty-five units, serial numbers 51 through 75, were submitted to HDL for mechanical shock on 15 August 1979 and returned to RCA/AS for end point testing. Twenty-five units, serial numbers 126 through 150, also were submitted to HDL on 15 August 1979 for gunfire environment. All units subjected to end point retesting passed the acceptance test requirements within specification. No replacement reserve units were used for substitute units.

Acceptance Test Report: The phase IV acceptance test report, in conformance with contract paragraph F.9.3, was submitted to HDL on 30 October 1979. This test report fully delineated the results of the test program along with the data generated during test.

Production Lot Balance: The 592 unit phase IV lot balance was completed and submitted to HDL on 30 October 1979.

Subgroup C1 - Gunfire Failure Analysis: As of the publication of this report, the 25 unit phase IV subgroup C1 test specimens had not been returned to RCA/AS for end point testing.

TABLE X - ACCEPTANCE TEST SAMPLE FLOW CHART/REQUIREMENTS

Subgroup/Flow	Qty.	Serial No.	Description	LTPD	MAN	AQL
ATS	174	1-158/R1-R16	Acceptance Test Sample	-	-	-
B5	8	R1-R8	Lead Integrity	30	0	0.64
B6	8	R9-R16	Solderability	30	0	0.64
A1	18	1-18	External Visual Insp.	20	1	2.0
A2	158	1-158	Operating Parameters	5	4	1.3
A3	25	1-25	High Temp. Performance	15	1	1.4
A4	25	1-25	Low Temp. Performance	15	1	1.4
B1	25	26-50	Temperature Cycling	15	1	1.4
B2	25	51-75	Mechanical Shock	15	1	1.4
B3	25	76-100	Constant Acceleration	15	1	1.4
B4	25	101-125	High Temp. Storage	15	1	1.4
C1	25	126-150	Gunfire	15	1	1.4
RR	8	150-158	Replacement Reserve			
EPR	125	26-150	End Point Retest			

2.4.4 Drawings

The engineering drawings and associated lists in conformance with CDRL sequence number A004 were completed with the submission of the following list of documents to HDL on 30 October 1979:

Drawing	Description	Rev.
A-11726754	Interface Circuit, Custom Monolithic Chip	B
D-11726759	Lead Frame Strip, 6 Position	0
C-11726760	Capacitor Chip, 820 pF, BX, 5%	0
D-11726761	Package Outline, Interface Hybrid Circuit	0
D-11726762	Assembly, Molded	0
D-11726763	Assembly, Premold	0
D-11726764	Substrate Assembly	0
D-11726765	Trimmed Substrate	0
C-11726766	Substrate, Laser-Scored, Interface Circuit	0
A-11726767	Substrate Ceramic, General Specification	0

Drawing A-11726755, Silicon Controlled Rectifier, Chip, Rev. B, was submitted to HDL on 20 November 1979.

2.4.5 Manufacturing Methods Notebook

The manufacturing methods notebook update, in conformance with contract paragraph F.9.6, is submitted along with this final report. The original notebook was initially submitted in phase II, in conformance with contract paragraph F.7.3, CDRL sequence A004. The current submission modifies that submission to reflect current status.

2.4.6 Special Tools

Three special dies were provided for phases III and IV. Advanced Plastics Machinery Corp. (APM), Ivyland, PA, designed and supplied all three dies which are now resident at RCA/AS, Burlington, MA. Although all three dies were provided as temporary tooling and are manual in operation, they are adequate for limited production quantities. The functional operations performed by these dies are quite simple and can be easily upgraded, by redesign, for high or extended production including automation as the need arises.

Lead Frame Preform Die: The lead frame preform die, a special die, is required to offset the leads in the six unit lead frame for acceptance of the substrate assembly prior to staking the substrate in place as shown in flow chart 12.

Lead Frame Staking Die: The lead frame staking die, a special die, is required to stake the substrate assembly in place for retention in the six unit lead frame prior to joining the substrate assembly and the lead drame with solder as shown in flow chart 12.

Lead Frame Cut and Forming Die: The lead frame cut and forming die, a special die, is required to separate the individual interface circuits from the six unit molded assembly, SCD 11726762, and to form the interface circuit leads in preparation for making as shown in flow chart 14.

Six Cavity Transfer Mold: Although a single cavity mold had been provided during phase II, the six cavity transfer mold was not used for phases III and IV. A six cavity transfer mold for use with the six unit premold assembly, SCD 11726763, was designed by Molding Technology, Inc. (MTI), Southampton, PA, and built by APM for use and in residence at RCA/SSD, Somerville, NJ. This six cavity transfer mold is suited for limited production quantities. However, minor design changes should be incorporated to improve the quality and yield of the transfer molded product.

Screens: Eight screens were provided for substrate fabrication during phases II, III, and IV, physically in residence at RCA/AS, Burlington, MA. These screens should be considered consumed.

2.4.7 Special Test Equipment

Special test equipment for phase IV, which was fully delineated in the test report of 16 January 1979, must be considered in two categories, in-line production test equipment and acceptance (environmental) test equipment.

In addition, in-line production test equipment is used at two stages of interface circuit production, first electrical test and final electrical test.

We discuss special test equipment in its normal operational sequence of use. In first electrical test, the substrate assembly is fully populated and is not encapsulated; in addition, no lead frame is installed.

Probe Card Adapter: The probe card adapter, a special test adapter, is a printed circuit card with 14 probes that interface with the substrate assembly lead frame attachment pads. This adapter acts as an interface between the substrate assembly and in-line test set BTA-2-2199. Although this probe card adapter is functionally adequate for limited production, redesign is required for high or continuous production to reduce its susceptibility to damage.

In-Line Test Set BTA-2-2199: In-Line Test Set BTA-2-2199, a special test set, was designed and provided by RCA/AS, Burlington, MA, in conformance with contract modification P00007 of 6 March 1979. It is a test set chassis used to interface with a Hewlett Packard 9825 computer. With the probe card adapter, it is used for first electrical test and final electrical test without the probe card adapter. All software is available for in-line production testing except for temperature subgroups A3 and A4. These subgroup requirements can be met with additional adapters and software. This test set is adequate for limited to medium or continuous production.

The acceptance test requirements were fulfilled on the RCA/AS EQUATE (AN/USM-410) test system which was fully delineated in the test report of 16 January 1979. For acceptance testing, three interface adapters were required. These are shown by figures 15 and 16.

Hybrid Interface Adapter: The hybrid interface adapter, a special test adapter, was designed to accept the 14 leads of this interface circuit.

Interface Test Cable: The interface test cable, a special test cable, is the interface between EQUATE (AN/USM-410) and the hybrid interface adapter.

Temperature Chamber Test Card: The temperature chamber test card, a special test adapter, is the interface between the interface circuit inside the temperature chamber and the hybrid interface adapter.

Since all of this equipment is used for acceptance testing only, although EQUATE (AN/USM-410) can be used for in-line production testing, the aforementioned special test equipment is fully adequate for acceptance testing needs.

Software: Software is available for all of the aforementioned special test equipment.

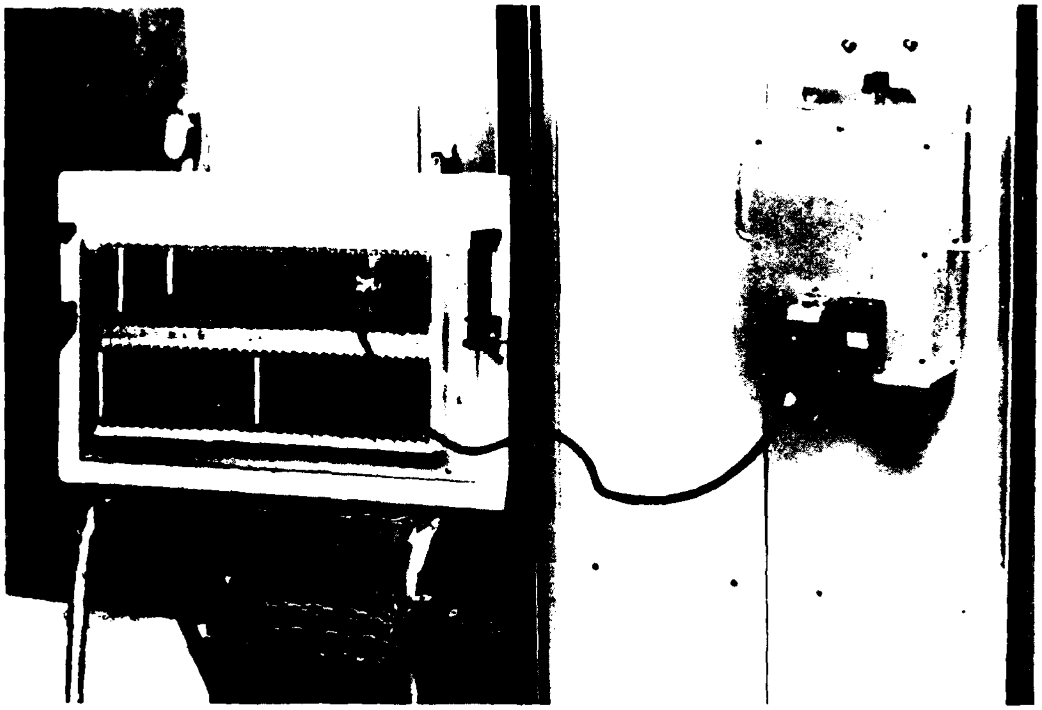


Figure 15. Acceptance Test Setup - Exterior

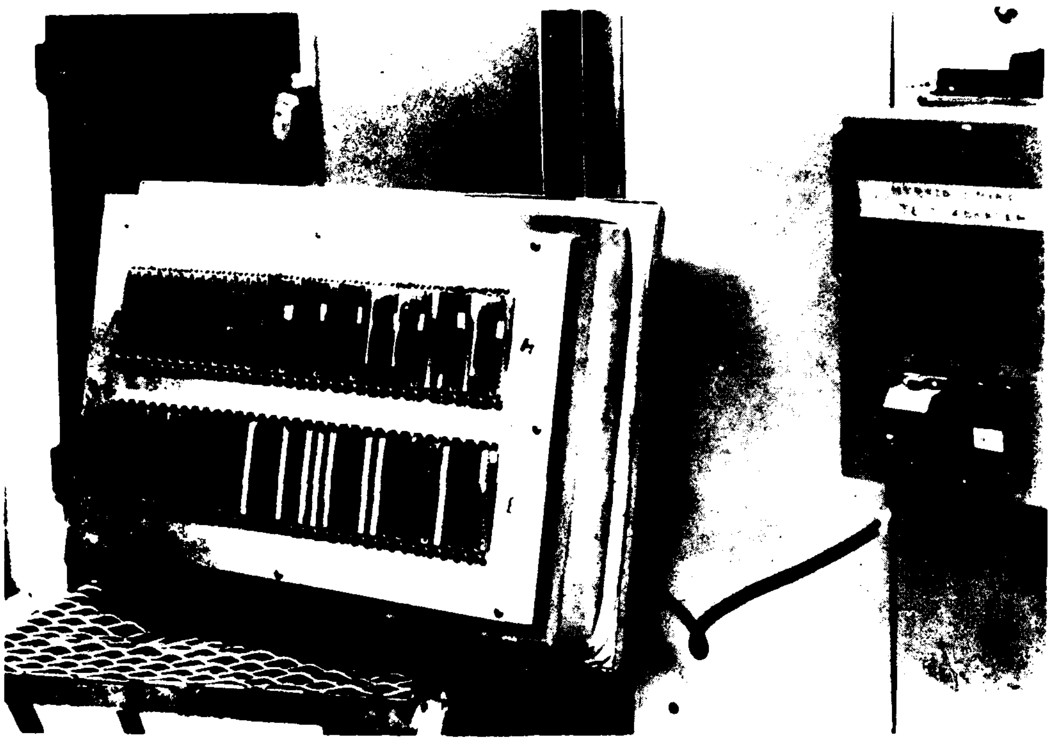


Figure 16. Acceptance Test Setup - Interior

2.4.8 Pilot Production Run Demonstrations

At various times during phase IV, process demonstrations of production techniques, procedures, and time studies were conducted to validate planning concepts. These demonstrations were conducted by RCA with HDL personnel in attandance.

On 1 February 1979, automatic screen printing was demonstrated at RCA/AS, Burlington, MA, for the glaze coating of the thick-film processing operations.

On 23 February 1979, laser trimming of the thick-film substrate resistors was demonstrated at RCA/SSD, Mountaintop, PA. Harry Diamond Laboratories personnel were not in attendance at this demonstration due to transportation difficulties, so a report was furnished.

On 9 to 11 April 1979, various substrate assembly techniques were demonstrated, such as solder dispensing, SCR placement, capacitor placement, IC placement, solder reflow, epoxy dispensing, and automatic wire bonding.

As discussed in the subsection Substrate Assembly Rework, the automatic wire bonder was not operating properly during the demonstration.

Production rates are discussed in section 4.

2.4.9 Special Process Instructions

The methods necessary to produce the interface circuit SCD 11726909 in general terms are not unique. Common, long established methods were designed into the product from the start. However for specific operations, specific details are obviously of assistance. Therefore, we have delineated these procedures with the following special process instructions, copies of which are available in the manufacturing methods notebook:

SPI-1017	Lead forming - interface circuit
SPI-1018	Staking - interface circuit
SPI-1019	Cut and form leads - interface circuit
SPI-2038	Transfer molding - interface circuit
SPI-2039	Surface preparation for marking
SPI-2040	Substrate to lead frame soldering

3. QUALITY ASSURANCE

RCA/AS, Burlington, MA, the prime contractor, and RCA/SSD, Somerville, NJ and Mountaintop, PA, maintain a quality assurance system in compliance with MIL-Q-50829, General Quality Assurance Provisions for Proximity Fuses and Related Components, and MIL-STD-883, Test Methods and Procedures for Microelectronics. For this HDL contract, quality assurance provisions have been in conformance to SCD 11726909 (section 4). In addition, RCA/AS, Burlington, MA has established internal quality assurance practices applicable to this program as follows:

- QP-237 Internal Visual (premold) Inspection of Hybrid Microcircuits
- QP-238 Hybrid Microcircuit Passive Substrate Visual Inspection
- QP-239 Marking and External Inspection of Hybrid Microcircuits
- QP-244 In-process Inspection of Hybrid Microcircuits
- QP-247 Control of Chip and Tab Mounting

4. COST ESTIMATE

Responding to SOW paragraph F.9.4, this section presents cost estimates for producing the interface circuit based upon data established during phase IV. Although the rates obtained at different manufacturing stations were discontinuous, they are applied here as if all operations were performed in continuous production with stations replicated as necessary to produce units at 110,000 per month. Also, the cost estimates assume one-shift operations of 8 hours per shift and a 5-day week.

One hundred ten thousand units per month convert to 636 units per hour for a 173 manhour month or 25434 units per 40-hour week. The level of equipment capitalization, the choice of lot size, and associated cycle time for the various production operations are interdependent. Consideration of these factors in depth for establishing an optimized production facilitation of machines and personnel would require extensive study. The optimization would, in particular, have to consider definitized yields at all points of manufacture, certainly fine tuned much better than the yields demonstrated during this program for the pilot production run.

But the cost estimate will attempt realistic use of the measured production rates and make a first-order approximation of the replication of equipment and operators necessary to maintain the 636-unit-per-hour production level. The estimate will reflect appropriate yields.

4.1 Cost-Estimating Model No. 1

The yields shown in table IX document what happened to the pilot lot through each major group of production operations. The "Yield from Net Start" column, showing cumulative yield, actually includes the yield improvement realized by those 185 units in sublot HDR01 that were reworked. But because of the fact that only a relatively small number of rejected units were reworked, the improved yield has no direct significance in establishing a cost-estimating model. The results of the rework are quantitatively significant in an indirect way for establishing a meaningful cost-estimating model as shown by figure 17. A reasonable prediction can be made relative to the effectiveness of the rework operation which is a basic part of the planned production process.

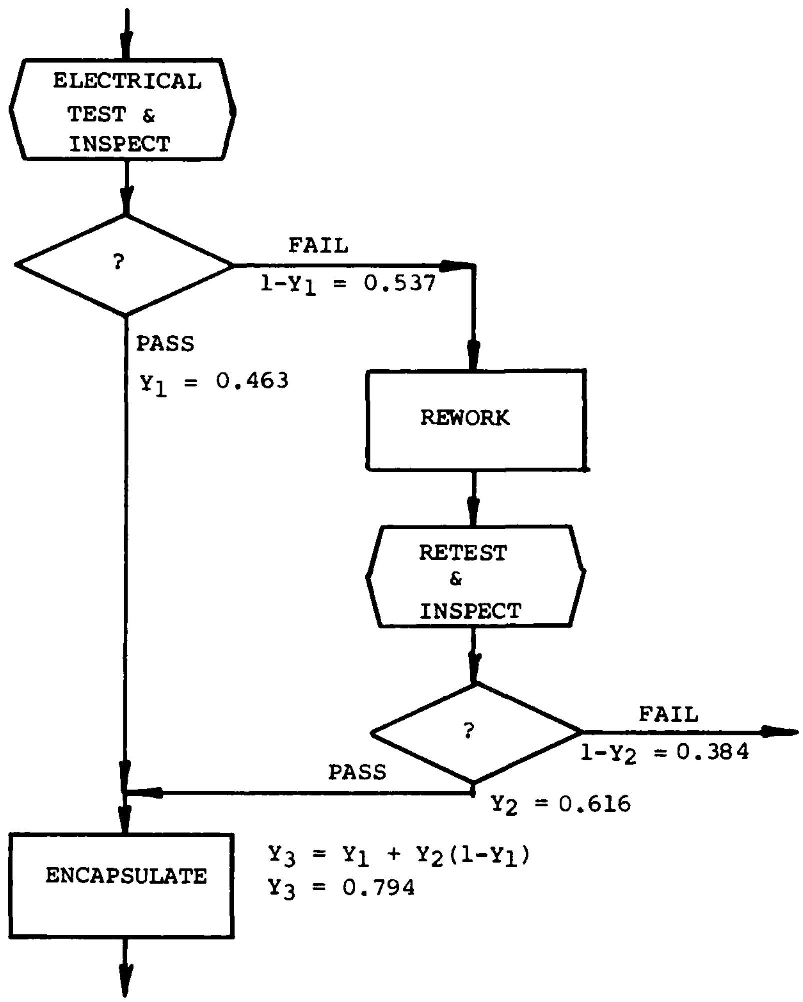


Figure 17. Yield Improvement with Rework

The effective yield of the composite group of operations made up of first electrical test, inspection, and rework is 79.4 percent. Furthermore, if all units that were rejected before encapsulation had been reworked, then the pilot lot record predictably would look like the adjusted table XI. The overall assembly yield instead of being 32.6 percent (a matter of record) would have been 57.3 percent and would still have reflected the effect of the chip damage from a hastily executed burnishing operation.

Although table XI was adjusted to reflect 100 percent rework of all initially rejected in-process units, it still gives a distorted view of yields, in particular for those operations following molding. Sixty four units, as recorded on the consolidated traveler for the shipping lot 7928, were deliberately marked red on one lead before molding to designate that they failed visual and mechanical requirements and in some cases merely filled out a six unit lead frame not completely populated with good substrates. The marking was supposed to flag them for immediate removal at the time that the molded units were cut away from the six unit lead frame assembly. Alas, instructions were not properly issued to operating personnel, and these units, known to be potentially bad, stayed with the lot until finally separated by a visual inspection after all testing was complete. Thus, they represent, by the actual record, a loss that should have been accounted for at lead-frame inspection or earlier. Table XI adjusts the yield story to show these units with red leads withdrawn from the lot during the group of operations associated with marking. This adjustment brings the overall assembly yield up to 61.2 percent. This table is used as cost-estimating model No. 1 for estimating yields.

4.2 Cost-Estimating Model No. 2

We must still ask how well the pilot lot might have proceeded had the thick-film gold been normal. RCA/AS has been successfully wire bonding a variety of hybrids using both manual and automatic equipment where the quantities of circuits are significantly larger than the phase IV lot quantity for the interface circuit, and the same thick-film gold is involved. It is appropriate to reexamine the records of assembly operations and attendant yields to establish a cost estimating model that adjusts for the burnishing misadventure. The [illegible] units were not burnished at all and thus not [illegible] scratching or any rework, then a first electrical test is practical (figure 18). Figure 17

TABLE XI - PRODUCTION QUANTITY AND YIELD DATA - ADJUSTED FOR 100% REWORK - PHASE IV

COST-ESTIMATING MODEL NO. 1

Production Process Operations	Quantity					Yield (%) from	
	Start	Sample Reserve	Net	Reject	Accept	Oper.	Net Start
Substrate Fabrication							
Thick-Film Processing	4420	120	4300	786	3514	81.7	81.7
Resistor Trimming	3514	0	3514	1133	2381	67.8	55.4
Hybrid Assembly							
Substrate Assembly	2381	3	2378	270	2108	88.6	88.6
1st Electrical Test/Inspect	2108	0	2108	2108	974	46.2	41.0
Rework	1404	0	1404	540	864	61.6	-
Encapsulation	1838	0	1838	0	1838	100.0	77.3
Lead Frame Assembly	1838	0	1838	41	1797	97.8	75.6
Molding	1797	0	1797	6	1791	99.7	75.3
Marking	1791	0	1791	15	1776	99.2	74.7
Final Electrical Test/Insp.	1776	0	1776	320	1456	82.0	61.2
Package and Ship	1456	-		0	1456	100.0	61.2

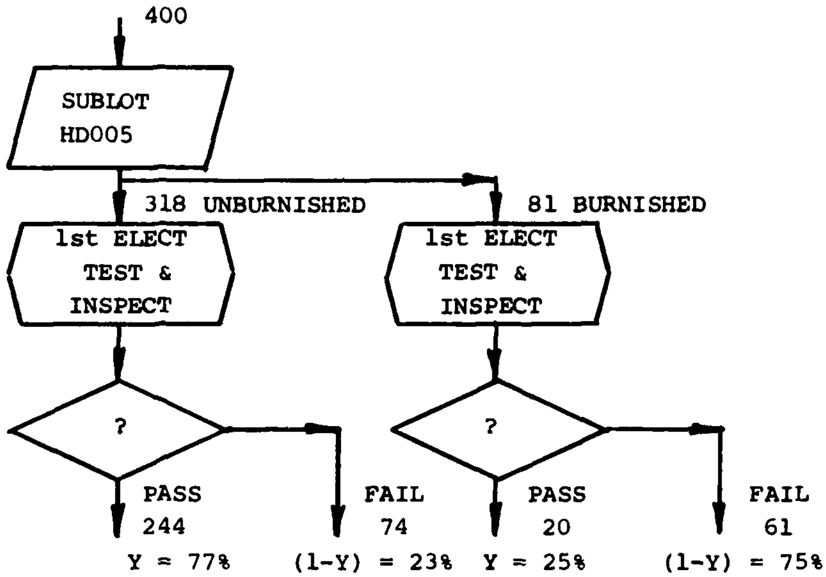


Figure 18. *Effects on Yield from Burnishing of Thick-Film Gold after Semiconductor Chip Assembly.*

could be redone to show Y1 = 77 percent, 1 - Y1 = 23 percent, Y2 = 62 percent, and Y3 = 91 percent. Y3 at 91 percent is the effective yield for the composite operation. The consolidated program traveler (table VIII) identifies 173 units lost at visual inspection after epoxy mounting the IC. This loss resulted mostly because of scratching of chip surfaces while eraser burnishing the thick-film gold. Had the burnishing not been done and assuming a loss of 20 units instead of 173, then the group of operations called substrate assembly would have had a demonstrated yield of 95 percent.

Table XII restates the pilot lot quantities and yields based on the assumption that the thick-film gold was normal and bondable and that the unplanned burnishing operation and accidental damage to chips did not take place. This adjustment brings the overall assembly yield up to 71.1 percent.

4.3 Other Yield Projections

Cost-estimating models No. 1 and No. 2 are both reasonable and based upon actual results derived from pilot production lot records and special tests. No attempt was made for either model to show yields other than those which are a matter of record. With experience, the yields in printing, drying, and firing would increase as indeed they would for laser trimming of resistors. Since such estimates would be speculative and not particularly illuminating, they are not presented at this time. In section 5, a number of recommendations are made to permit ready improvement of yields from the baseline demonstrated during this program.

4.4 Production Rates

Rates established during pilot production are provided by table XIII for substrate fabrication and by tables XIV and XV for assembly operations before and after encapsulation, respectively. These rate charts along with the cost-estimating model charts become the basis for realistic estimates of hybrid costs in high volume. The labor hours derivable from this information establish the direct, hands-on labor, omitting the supervision and technical support essential to keeping the work flowing smoothly and in maintaining and setting up equipment for optimized, uninterrupted manufacture. This additional labor will be estimated separately and added to the basic labor for the manufacturing operations.

TABLE XII - PRODUCTION QUANTITY AND YIELD DATA - ADJUSTED FOR NO BURNISHING - PHASE IV
COST ESTIMATING MODEL NO. 2

Production Process Operations	Quantity					Yield (%) from	
	Start	Sample Reserve	Net	Reject	Accept	Oper.	Start
Substrate Fabrication							
Thick-Film Processing	4420	120	4300	786	3514	81.7	81.7
Resistor Trimming	3514	0	3514	1133	2381	67.8	55.4
Hybrid Assembly							
Substrate Assembly	2381	0	2381	120	2261	95.0	95.0
1st Electrical Test/Inspect	2261	0	2261	521	1740	77.0	73.1
Rework	641	0	641	245	396	61.9	-
Encapsulation	2136	0	2136	0	2136	100.0	89.7
Lead Frame Assembly	2136	0	2136	47	2089	97.8	87.7
Molding	2089	0	2089	7	2082	99.7	87.4
Marking	2082	0	2082	17	2065	99.2	86.7
Final Electrical Test/Insp.	2065	0	2065	372	1693	82.0	71.1
Package and Ship	1693	0	1693	0	1693	100.0	71.1

TABLE XIII - COST ESTIMATING DATA - SUBSTRATE FABRICATION RATES

Oper. Seq. No.	Yield Factors for Cost Model No. 1	Yield Factors for Cost Model No. 2	Operation	Rate (Circuits per hr)	No. of Operators	Equipment Used Type	Equipment Used Qty
1	2.95	2.54	Clean Scored Plates	4800	1		
2	2.95	2.54	Print/Dry Pt-Au	8000	1	Printer/Dryer #1	1
3	2.95	2.54	Fire Pt-Au	4000 x 2	1	Furnaces #1&2 (8")	2
4	2.95	2.54	Print/Dry Au	8000	1	Printer/Dryer #1	1
5	2.95	2.54	Fire Au	4000 x 2	1	Furnaces #1&2	2
6	2.95	2.54	Print/Dry 300K/sq.	8000	1	Printer/Dryer #2	1
7	2.95	2.54	Print/Dry 30K/sq.	8000	1	Printer/Dryer #2	1
8	2.95	2.54	Print/Dry 3K/sq.	8000	1	Printer/Dryer #2	1
9	2.95	2.54	Print/Dry 300/sq.	8000	1	Printer/Dryer #2	1
10	2.95	2.54	Fire Resistors	4000 x 2	1	Furnaces #1&2	2
11	2.95	2.54	Print/Dry Glaze	8000	1	Printer/Dryer #1	1
12	2.95	2.54	Fire Glaze	4000 x 2	1	Furnaces #1&2	2
13	2.41	2.08	Burnish	120	11	Manual Sta. (eraser)	11
14	2.41	2.08	Snap Scored Plates	1200	1	Manual	1
15	2.41	2.08	Clean	240	6	-	6
16	2.41	2.08	Laser Trim Resistors	240	6	RCA Mountaintop, Pa.	6
17	2.41	2.08	Clean	240	6	-	6
18	2.41	2.08	Inspect	240	6	Microscope	6
19	2.41	2.08	QC Inspect	-	-	Microscope	-

TABLE XIV - COST ESTIMATING DATA - PREENCAPSULATION ASSEMBLY RATES

Oper. Seq. No.	Yield Factors for Cost Model		Operation	Rate (Circuits per hr)	No. of Oper- ators	Equipment Used	
	No. 1	No. 2				Type	Qty
20	1.70	1.45	Eutectic Bond SCR Chip to Molytab and Clean	50	20	Die Bonder	20
21	1.70	1.45	Visual Inspect	900	1	Microscope	1
22	1.63	1.41	Apply Solder Paste	150	6	Laurier Dispenser	6
23	1.63	1.41	Mount Capacitor and SCR Chip-Tab	140	7	Manual Station	7
24	1.63	1.41	Reflow Solder/Dlean Flux	600	2	Browne Rotary	2
25	1.63	1.41	Vis.Inspect Solder Oper.	360	3	Microscope	3
26	1.63	1.41	Apply Epoxy	483	2	Laurier Dispenser	2
27	1.63	1.41	Mt. IC Chip/Cure Epoxy	230	4	Manual Station/Oven	4/1
28	1.63	1.41	Vis.Inspect Epoxy Oper.	360	3	Microscope	3
29	1.63	1.41	QC Sample Inspect	-	-	-	-
30	1.63	1.41	Cobehn Spray Clean	360	3	Cobehn Sprayer	3
31	1.63	1.41	Wire Bond	48	19	GCA Auto Wirebonder	19
32	1.63	1.41	100% Visual Inspect	180	5	Microscope	5
33	1.45	1.34	100% Electrical Test	180	5	Probe Sta./Auto Tester	5
34	1.45	1.34	QC Inspect	90	10	Microscope	10
35A	0.96	0.38	Rework: Define Rework	30	8	Records & Microscope	8
35B	0.96	0.38	Rework, Retest and Inspect	17	15	Variety	15

TABLE XV - COST ESTIMATING DATA - FINAL ASSEMBLY RATES

Oper. Seq.	Yield Factors for Cost Model		Operation	Rate (Circuits per hr)	No.of Oper. ators	Equipment Used	
	No. 1	No. 2				Type	Qty
36	1.26	1.26	Epoxy Coat Chips/Cure	75	11	Manual Sta./Oven	11/1
37	1.26	1.26	Preform Lead Frame Assembly	380	2	Preform Die	2
38	1.26	1.26	Stake Substrates in Lead Frame	380	2	Staking Die	2
39	1.26	1.26	Apply Solder Paste	150	6	Manual Sta.	6
40	1.26	1.26	Reflow Solder	300	3	Hot Plate	3
41	1.26	1.26	Remove Flux/Clean	300	3	Manual Sta.	3
42	1.26	1.26	QC Inspect	300	3	Microscope	3
43	1.26	1.26	Transfer Mold	60	1	6-Cavity Mold	14
44	1.26	1.26	Visual Inspect	1200	1	Microscope	1
45	1.23	1.23	Cut & Form Leads/Inspect	134	6	Die sets/press	6
46	1.23	1.23	Prepare Surface for Marking	120	7	Manual Sta.	7
47	1.23	1.23	Mark/Cure/Inspect	120	7	Manual Markem	7
48	1.22	1.22	Final Electrical Test	300	3	Auto.Test Sta.	3
49	1.00	1.00	QC Inspect	300	2	Microscope	2
				TOTAL	218		

Yield factors are provided in the rate charts (tables XIII to XV). These values were determined from a division of the appropriate start quantity by the final completed quantity on the charts of cost-estimating models No. 1 and No. 2 (tables XI and XII).

Table XVI gives the backup detail to support the labor content estimated for rework (operation sequence No. 35).

4.5 Replication of Equipment and Work Stations

The production rate charts also include estimates of the number of operators and equipment (or work stations) that are required to support the delivery of 110,000 hybrids per month for cost estimating model No. 2. To estimate the replication needs for assembly was quite straightforward; but to do so for the thick-film printing, drying, and firing operations required a review of the systematic type scheduling that would be necessary to make efficient use of equipment. Figure 19 shows one possible way in which production lots might be scheduled to satisfy the high production rate requirements. In this illustration, two printer-dryer complexes are employed. One printer-dryer complex is dedicated to resistor printing of the four layers of different resistivities. A second printer-dryer complex is used for the two conductor layers and the glaze layer. The simple arithmetic supporting this arrangement is as follows:

Substrate fabrication yield factor:	2.54
Composite resistor printer-dryer rate rate (four layers):	2000 circuits/hr
Final product delivery rate:	110,000 circuits/mo

$$\frac{110{,}000\ (2.54}{2{,}000} = 140\ \text{hr/mo}$$

$$\frac{140\ \text{hr/mo}}{173\ \text{hr/mo}} \times 100 = 81\%$$ (not counting setup and maintenance times)

Composite conductor/glaze rate (three layers): 2700 circuits/hr

$$\frac{110{,}000\ (2.54)}{2{,}700} = 103\ \text{hr/mo}$$

$$\frac{103\ \text{hr/mo}}{173\ \text{hr/mo}} \times 100 = 59\%$$ (not including setup and maintenance times)

TABLE XVI - COST ESTIMATING DATA - REWORK LABOR RATES

Operation Seq. No.	Rework Operation	Rate (circuits/hr)	Operation Time (circuits/hr)
35	Define Rework	30	33.3E-3
35B	Perform Rework		
	Remove IC*	120	8.3E-3
	Apply Epoxy	483	2.1E-3
	Mount IC	230	4.3E-3
	Visual Inspect	360	2.8E-3
	Cobehn Clean	360	2.8E-3
	Wire Bond	65	15.4E-3
	Visual Inspect	180	5.6E-3
	Retest	180	5.6E-3
	Visual Inspect	90	11.1E-3
	Composite	17.3	57.9E-3
35	Overall Rework	11	91.2E-3

*Typical rework and most costly

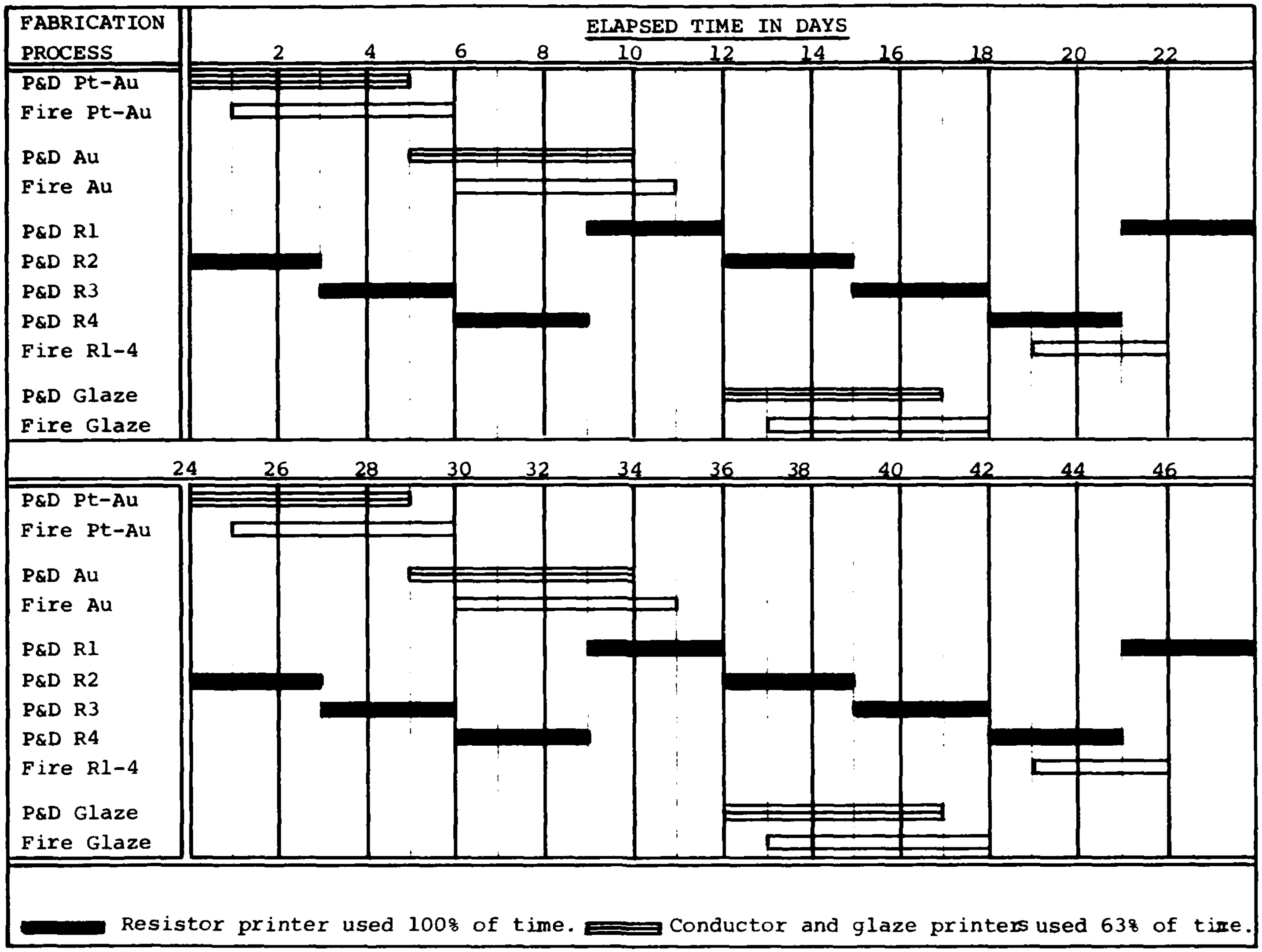


Figure 19. Representative Substrate Fabrication Lot Formation Schedule

4.6 Labor

Tables XVII to XIX present the calculated yielded labor for all operations in substrate fabrication and assembly. The labor is given in terms of manhours per 1000 units deliverable. These tables help to highlight those operations with high labor content as follows:

- No. 13 eraser burnish platinum gold for improved solderability
- No. 20 eutectic bonding of SCR chip to gold-plated molybdenum tab
- No. 31 wire bonding
- No. 35 rework of IC chips
- No. 36 epoxy coating of chips and wires in preparation for molding
- No. 43 transfer molding

Comments relative to some of these operations may be found in section 5.

Labor hours are given for convenience on the basis of 1000 deliverable units. Table XVII delineates labor for substrate fabrication: table XVIII, preencapsulation assembly; and table XIX, final assembly.

4.7 Material

High-volume material estimates are given in table XX. The first column shows the basic material cost for each item as applied to 1000 circuits. By multiplying these figures by the yield factors in the next two columns for the appropriate cost-estimating model, one comes up with the yielded material cost by item for 1000 deliverable units. The thick-film, noble-conductor costs loom large in today's gold market, strongly motivating use of less costly material. The material costs are based upon a purchase appropriate to delivery of about 250,000 units.

TABLE XVII - COST ESTIMATING DATA - SUBSTRATE FABRICATION DATA

Oper. Seq. No.	Yielded Labor per Operation for Each 1000 Units Deliverable		Yielded Cumulative Labor per 1000 Units Deliverable	
	Cost Est. Model No. 1 (hr)	Cost Est. Model No. 2 (hr)	Cost Est. Model No. 1 (hr)	Cost Est. Model No. 2 (hr)
1	.61	.53	.61	.53
2	.37	.32	.98	.85
3	.37	.32	1.35	1.16
4	.37	.32	1.72	1.48
5	.37	.32	2.09	1.80
6	.37	.32	2.46	2.12
7	.37	.32	2.83	2.43
8	.37	.32	3.20	2.75
9	.37	.32	3.56	3.07
10	.37	.32	3.93	3.39
11	.37	.32	4.30	3.37
12	.37	.32	4.67	4.02
13	20.08	17.33	24.75	21.36
14	2.01	1.73	26.76	23.09
15	10.04	8.67	36.80	31.76
16	10.04	8.67	46.85	40.42
17	10.04	8.67	56.89	49.09
18	10.04	8.67	66.93	57.76

TABLE XVIII - COST ESTIMATING DATA - PREENCAPSULATION LABOR

Oper. Seq. No.	Labor per Operation for Each 1000 Units Deliverable		Cumulative Labor per 1000 Units Deliverable	
	Cost Est. Model No. 1 (hr)	Cost Est. Model No. 2 (hr)	Cost Est. Model No. 1 (hr)	Cost Est. Model No. 2 (hr)
20	34.00	29.00	34.00	29.00
21	1.89	1.61	35.89	30.61
22	10.87	9.40	46.76	40.01
23	11.64	10.07	58.40	50.08
24	2.72	2.35	61.12	52.43
25	4.53	3.92	65.64	56.35
26	3.37	2.92	69.02	59.27
27	7.09	6.13	76.10	65.40
28	4.53	3.92	80.63	69.32
29	-	-	-	-
30	4.53	3.92	85.16	73.23
31	33.95	29.38	119.12	102.61
32	9.06	7.83	128.17	110.44
33	8.06	7.44	136.23	117.89
34	16.11	14.89	152.34	132.77
35A	32.00	12.67	184.34	145.44
35B	56.47	22.35	240.81	167.79

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INTERFACE CIRCUIT 11726909 MATERIALS, METHODS, AND TECHNOLOGY P--ETC(U)
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TABLE XIX - COST ESTIMATING DATA - FINAL ASSEMBLY LABOR

	Labor per Operation for Each 1000 Units Deliverable		Cumulative Labor per 1000 Units Deliverable	
Oper. Seq. No.	Cost Est. Model No. 1 (hr)	Cost Est. Model No. 2 (hr)	Cost Est. Model No. 1 (hr)	Cost Est. Model No. 2 (hr)
36	16.80	16.80	16.80	16.80
37	3.32	3.32	20.12	20.12
38	3.32	3.32	23.43	23.43
39	8.40	8.40	31.83	31.83
40	4.20	4.20	36.03	36.03
41	4.20	4.20	40.23	40.23
42	4.20	4.20	44.43	44.43
43	21.00	21.00	65.43	65.43
44	1.05	1.05	66.48	66.48
45	9.18	9.18	75.66	75.66
46	10.25	10.25	85.91	85.91
47	10.25	10.25	96.16	96.16
48	4.07	4.07	100.23	100.23
49	3.33	3.33	103.56	103.56

TABLE XX - COST ESTIMATING DATA - MATERIAL

Material Description	Cost/1000 Circuits	Yield Factor for Cost Model		Yielded Cost/1000 Circuits for Cost Model	
		No. 1	No. 2	No. 1	No. 2
11726766 Laser Scored Substrates	$ 43	2.95	2.54	145	124
Platinum Gold & Gold Inks @ $14.00/g	644	2.95	2.54	1900	1636
Resistor Inks @ $4.90/g	15	2.95	2.54	44	38
Glaze Ink @ $1.00/g	5	2.95	2.54	15	13
.06 x .06 x .005 Gold-Plated Molytab	60	1.70	1.45	102	87
11726760 Chip Capacitor	58	1.63	1.41	95	82
11726755 SCR Chip	1000	1.63	1.41	1630	1410
11726754 IC Chip	1450	1.63	1.41	2364	2045
Rework Chips		.96	.38	1392	551
11726759 Lead Frame	141	1.26	1.26	178	178
Misc. Potting Pastes & Ink	100	1.3	1.3	130	130
	Total Purchased Material			$ 7995	$ 6294

Note: Except for specified ink prices, other material prices are based on those in effect on April 1979.

4.8 Unit Cost Calculations

Drawing upon all of the cost-estimating data introduced in the preceding paragraphs, tables XXI and XXII develop and summarize the results leading to the projected unit costs for the interface circuit being produced at the rate of 110,000 deliverable units per month.

Cost-estimating model No. 1 - \$15.58 per unit

Cost-estimating model No. 2 - \$12.30 per unit

These tables show the addition of supervisory, technical, and quality assurance labor, especially important in the management, setup, and maintenance of automated equipment and production lines. Although labor costs do include overhead, and material costs do reflect a material handling expense, the unit costs do not include General and Administrative (G&A), Independent Research and Development (IR&D), or profit. Overheaded labor costs are based upon RCA manufacturing rates in effect in December 1979.

4.9 Cost Projections

The SOW says that a basic objective of this MM&T program is "to define manufacturing methods capable of fabricating 110,000 devices/ month at a cost of less than four dollars each (average price fcr the third million)".

Based upon measured production rates, yields, and current material estimates, we have shown that we can reasonably expect to produce the interface circuit at a unit cost of \$12.30. But how do we reconcile \$12.30 with the \$4.00 objective stated above?

First, let us bring the \$4.00 up to date by using the dollars of today instead of the dollars of 1977, when the SOW was issued. Four dollars becomes about \$5.00 because of inflation. We can cry a little about our choice of gold and platinum gold in the thick-film conductor system, since now these noble conductors represent 26 percent of the material cost instead of the 10 percent that they represented a few years ago when the choice was made.

TABLE XXI - SUMMARY COSTS: ESTIMATING MODEL NO. 1

Description	Yielded Labor (hr/1000)		Yielded Material ($/1000)	Unit Cost ($/Unit)
Substrate Fabrication	67		2104	
Preencapsulation Assembly	241		5841	
Final Assembly and Test	104		50	
Total Operator Labor		412		
Supervision (15%)	62			
Engineering Support (5%)	21			
Mat'l Control & Admin. (5%)	21			
Quality Assurance (5%)	21			
Total Supervision/Support		125		
Total Direct Labor Hours		537		
Unit Labor Cost (with O.H.)				7.08
Purchased Material			7995	
MHX (6.3%)			504	
Total Material			8499	
Unit Material Cost				8.50
Total Unit Cost				$ 15.58

TABLE XXII - SUMMARY COSTS: ESTIMATING MODEL NO. 2

Description	Yielded Labor (hr/1000)		Yielded Material ($/1000)	Unit Cost ($/Unit)
Substrate Fabrication	58		1811	
Preencapsulation Assembly	168		4433	
Final Assembly and Test	104		50	
Total Operator Labor		330		
Supervision (15%)	50			
Engineering Support (5%)	16			
Mat'l Control & Admin. (5%)	16			
Quality Assurance (5%)	16			
Total Supervision/Support		98		
Total Direct Labor Hours		428		
Unit Labor Cost				5.6[illegible]
Purchased Material			6294	
MHX (6.3%)			397	
Total Material			6691	
Unit Material Cost				6.6[illegible]
Total Unit Cost				$ 12.3[illegible]

The \$12.30 cost figure for producing the hybrid at a rate of 110,000 units per month is conservatively high because it reflects the relative immaturity of the new processes being used as well as the inexperience of the personnel involved. Therefore, it makes good sense to use the classical experience curve (also called the learning curve) to predict the probable average unit cost for the production of the third million.

4.9.1 Learning Curve

The learning curve shows the relationship of the cost of a given unit to the cumulative number of units produced in accordance with the following simple formula:

$$\frac{C_2}{C_1} = \left(\frac{N_2}{N_1}\right)^a \qquad (1)$$

$$\text{or } \log \frac{C_2}{C_1} = a \log \frac{N_2}{N_1} \qquad (2)$$

where C_2 is the cost of unit number N_2, and C_1 is the cost of unit number N_1. When C_2/C_1 and N_2/N_1 are plotted on log-log paper, the curve plots as a straight line. One can describe the slope of this line in terms of the percentage of reduction realized in the normalized quantity N_2/N_1. The exponent "a" is related to this slope by the following expression:

$$\text{Slope (\%)} = 2^a \times 100\% \qquad (3)$$

or

$$a = \frac{\log \left[\dfrac{\text{Slope (\%)}}{100\ \%}\right]}{\log 2} \qquad (4)$$

For large quantities of units, a very close approximation of the average can be calculated by using integration of the learning curve:

$$C_{AV} = \frac{C_1}{N_1{}^a (N_2 - N_1)} \int_{N_1}^{N_2} N^a dN \qquad (5)$$

$$C_{AV} = \frac{1}{N_2 - N_1} \frac{C_1}{a+1} \left[\left(\frac{N_2}{N_1}\right)^a N_2 - N_1 \right] \qquad (6)$$

Although tedious computer-generated tables are available for use in manipulating the various combinations of learning-curve slopes, quantities, and costs, the programmable calculator permits ready exercising of the variables, with calculations based upon equations (1), (4), and (6) above.

4.9.2 Results of Calculations

As summarized by table XXII, the unit cost predicted by measured rates and measured and adjusted yields was $12.30. Five dollars and sixty-one cents of this was the labor cost, and $6.69, the material cost. In order to make use of the learning curve, we have made the assumption that these cost figures apply specifically to the cost for unit number 110,000. The slope for labor is not necessarily the same as the slope for material. In particular, if the material being used is standard and is used in large quantity by other people, then the volume production and large-quantity purchase for the interface circuit will not do much to drive material costs down; however, the custom IC costs would be affected by high volume procurement. Basic improvements in yields, of course would drive down significantly the effective, yielded cost of all material.

Table XXIII looks at the projected costs of material and labor independently for learning-curve slopes from 75 percent to 100 percent in 5-percent steps. Here we see the calculated material and labor costs for the two-millionth unit and the three-millionth unit along with the average cost for the entire third million units produced.

Table XXIV takes these data and presents the total average unit cost in the form of a matrix uniting the learning-curve slopes for material with corresponding learning-curve slopes for labor. The reader may use his own judgment in estimating the future cost of the interface circuit. If he believes material can reasonably be expected tc follow a 90-percent slope and labor a 75-percent slope, then he can find the projected unit cost to be $5.70, somewhat above the goal of $5.00 per unit. But should he assume an 85-percent slope for material, the projected unit cost would be $4.76, somewhat less than $5.00 per unit.

Table XXV presents the labor and material costs and slopes from a different point of view. Here we answer the questions, "What combinations of calculated material and labor costs and associated learning-curve slopes will lead to an average unit cost of $5.00? How does labor compare on a percentage basis with the total cost?" A rather limited

range of slopes for material (80 to 85 percent) is shown in the table. This range of slopes and associated material costs leads to believable labor slopes and costs with the percentage of labor cost to total cost coming out between 35 and 51 percent.

4.9.3 Conclusion

The use of learning-curve projections has demonstrated that the $5.00 average cost figure for the third million of production hybrids is basically realizable by using the manufacturing methods and technology of this program. This expectation could be assured by further process improvements and material adjustments recommended in section 5.

TABLE XXIII - LEARNING CURVE CALCULATIONS FOR MATERIAL AND LABOR UNIT COST

Slope of Learning Curve (%)	Material ($)			Labor ($)		
	Cost of Unit No.		3rd Million Average	Cost of Unit No.		3rd Million Average
	2×10^6	3×10^6		2×10^6	3×10^6	
100	6.69	6.69	6.69	5.61	5.61	5.61
95	5.40	5.24	5.31	4.53	4.39	4.45
90	4.30	4.05	4.16	3.61	3.39	3.49
85	3.39	3.08	3.22	2.84	2.58	2.70
80	2.63	2.31	2.45	2.21	1.94	2.06
75	2.01	1.70	1.84	1.68	1.42	1.54

TABLE XXIV - AVERAGE UNIT COST FOR THIRD MILLION USING LEARNING CURVE

		Slope (%) for Material					
		100	95	90	85	80	75
Slope (%) for Labor	100	12.30	10.92	9.77	8.83	8.06	7.45
	95	11.14	9.76	8.61	7.67	6.90	6.29
	90	10.18	8.80	7.65	6.71	5.94	5.33
	85	9.39	8.01	6.86	5.92	5.15	4.54
	80	8.75	7.37	6.22	5.28	4.51	3.90
	75	8.23	6.85	5.70	4.76	3.99	3.38

TABLE XXV - LABOR AND MATERIAL COSTS AND SLOPES FOR CALCULATED AVERAGE UNIT COST OF $5.00

Material Cost		Labor Cost			Total Average for 3rd Million ($)
Slope (%)	3rd Million Average ($)	Slope (%)	3rd Million Average ($)	Percentage of Total	
85	3.22	77.5	1.78	35.6	5.00
84	3.06	79.0	1.94	38.9	5.00
83	2.90	80.4	2.10	42.1	5.00
82	2.74	81.7	2.26	45.2	5.00
81	2.60	82.8	2.40	48.1	5.00
80	2.45	83.9	2.55	51.0	5.00

5. RECOMMENDATIONS

Time now for that 20-20 look behind at where we have been so perhaps we can see ahead clearer to where we would like to go. Experience with the product in a simulated production environment has given new insight to both designer and builder. In the following paragraphs, recommendations are made in those areas where clear direction is indicated, and problems are highlighted even if no clear solutions are evident. No attempt is made to present comments in any particular order of priority or urgency. Instead, observations are made as a result of reviewing the process flow drawing starting with the bare substrate and ending with the deliverable hybrid.

5.1 Laser Scored Substrate

Consideration should be given to laser scoring the back side of the substrate instead of the front side. Doing so would avoid contamination of the surface from debris of the scoring process. Some debris, almost invisible under the microscope, deposited as a mist as far away as 0.1 in. from the glassy kerf region of the basic laser scored line causes poor adhesion of deposited gold in those regions. More vigorous abrasive cleaning can minimize the problem as can better control of the laser scoring process.

5.2 Multiimage Pattern Location on Substrate

The 20-image pattern as now specified fits on a 3 x 3 in. ceramic plate with eight of the circuits running along two edges of the plate. Uniformity of printing could be improved by shifting the entire pattern so that the five vertical circuits are symmetrical with the horizontal axis. Two equal borders of bare ceramic are then along the top and bottom edges, The right-hand side can still be the boundary of the five vertical circuit images along that edge. The top and bottom borders will act as supports for the printing squeegee as it moves from left to right in each printing operation.

5.3 Backside Platinum Gold

Printing on the back with platinum gold is unnecessary. Originally it had been planned to solder the lead frame on both the back and the front of the substrate for extra mechanical strength. The combination of the staking operation of the lead frame itself, the soldering

on the front, and finally the complete solid molding adequately secures the lead frame to the substrate as confirmed by the successful environmental exercises that the finished product has been subjected to. The cost estimates did not include consideration of backside conductor printing even though it was done.

5.4 Conductor Systems

In a way, this hybrid product clearly departed from a low-cost approach when platinum gold and gold metal systems were used for solder pads and conductor runs instead of silver palladium or other suitable lower cost conductor systems that have been successfully applied to other nonhermetic, encapsulated hybrids used in fuzes. Here, 20-20 vision gets really sharp as gold prices soar. Perhaps a compromise might be made in which gold is used just for wire-bond pads to improve yield on that critical process, but a less expensive conductor is used for all other runs.

5.5 Resistor Probe Pads

The laser trimming of resistors was handicapped by poor (no) contacting of some of the resistors. This problem would be reduced by making larger probe pads where possible and by opening up the encroaching glaze patterns in the regions where probing is planned.

5.6 Glaze Layer

The glaze layer represents an overkill. Glaze on this circuit can be significantly and advantageously reduced. It can be removed from the top of all resistors, improving laser trimming.

5.7 Laser Trimming

Laser trimming of resistors can be obviously reduced by trimming before snapping the substrates apart into 20 separate circuits. Individual substrate trimming reflected by the process flow and by the cost estimate was accomplished only as an expediency on this program because of the readily available use of the RCA individual substrate trimming system at Mountaintop, PA.

5.8 Snapping of Laser-Scored Substrate

Additional tooling should be designed to automate the snapping process for separating individual circuits from the four by five matrix.

5.9 Burnishing of Conductors for Solderability

Because burnishing of conductors for solderability is burdensome, it really needs improvement or elimination. Perhaps the change to the metal conductor system recommended in section 5.4 can solve this solderability problem at the same time.

5.10 Eutectic Bonding of SCR Chip

The process now used is one of bonding the SCR semiconductor chip eutectically to the gold-plated molybdenum tab. This chip mounting is slow and expensive in its present manual form. This program did not address any effort toward automating the process although some ideas involving automatic feed of the tabs was considered. When looking at this process, we must also consider subsequent processes and those places where we may make improvements.

In particular, we found that the solder-mounted capacitor and the solder-mounted chip-tab assembly both reflowed once more at the time that the solder on the lead frame pads was reflowed. This additional reflow coupled with two exposures to high temperature epoxy curing cycles led to degradation of the solder joints. One might ask, "Why not eliminate the solder altogether?" Indeed, this is a reasonable question in light of experience. For consideration, therefore, is a proposal to eutectically mount the SCR chip directly on thick-film gold of the substrate and then, instead of using solder to attach the chip capacitor, use conductive epoxy at the same time that the custom IC is mounted also with conductive epoxy. And so we eliminate the soldering operation and the attendant flux removal cleaning steps as well. The chip capacitor is located in a high resistance circuit where the somewhat variable contact resistance of conductive epoxy would not be noticeable in the electrical performance of the circuit.

5.11 Custom IC Chip Surface Protection

The specification for the custom IC chip should be revised to specify a glassivation layer to protect the surface from scratching and other damage.

5.12 Lead Frame Soldering

During the pilot production run, the process for soldering had to shift from furnace reflow to hot plate reflow to avoid the excess secondary reflow of the previously soldered capacitor and chip-tab assembly. (See also section 5.10.) For reasons not yet apparent, it might not be practical to eutectically mount the SCR chip directly to thick-film gold and epoxy mount the capacitor. Then another approach could be readily implemented following the original process of solder mounting these parts and later soldering the lead frame in the furnace. This approach could be done reliably by merely changing the solder used for the chips from 62-36-2 Sn-Pb-Ag to 10-90 Sn-Pb, which has its liquidus at 300°C. We actually came close to doing this at an earlier point in the program when difficulties were encountered in the molding process and higher mold temperatures were being considered.

5.13 Transfer Molding

Some minor design changes are necessary in the multiple-cavity mold to improve the venting and avoid losses due to voiding. In high volume production, the present 6-cavity mold should be replaced by a 48-cavity mold to increase the production rate.

5.14 Preparation for Marking

The silicone molding material does not mark well unless the surface is roughed up. It was roughed up by a manual sanding operation on this program. This process needs to be automated and better controlled.

5.15 Marking

The marking ink used for this job was a single component epoxy ink. The curing temperature was 150°C. Some circuit losses can be attributed to the marking operation and the thermal stresses to the final product. Whether these attributions are valid or not, the circuit could be marked equally well with a two-component epoxy ink that would not require a high (potentially stressful) curing temperature.

APPENDIX A. PHASE III - FIRST ARTICLE ACCEPTANCE SAMPLE

Appendix A consists of table Al which provides the "before" variables data, and table A-2 which provides the "after" variables data for the phase III acceptance test subgroup Cl gunfire test specimens.

TABLE A-I - BEFORE SUBGROUP C1 ACCEPTANCE TEST

TEST DATA - X5597 [illegible] PAGE 1 OF 9
CONTRACT NO.
SUBGROUP C-1 ([illegible])
LOT NO. 7844

NOTES	IR6 1	IR6 2	IR10 1	IR10 2	IR16 1	IR16 2	IR5 1	IR5 2
UNIT NO.-DATE CODE								
126-7843	0.46	0.00	7.45	0.00	2.03	0.06	0.90	0.00
127-7844	0.46	0.00	7.41	0.00	2.02	0.00	0.90	0.00
128-7844	0.46	0.00	7.41	0.00	2.02	0.00	0.90	0.00
129-7844	0.46	0.00	7.57	0.00	2.02	0.00	0.90	0.00
130-7844	0.46	0.00	7.41	0.00	2.02	0.00	0.90	0.00
131-7844	0.46	0.00	7.42	0.00	2.03	0.00	0.90	0.00
132-7844	0.46	0.00	7.42	0.00	2.03	0.00	0.90	0.00
133-7844	0.46	0.00	7.41	0.00	2.02	0.00	0.90	0.00
134-7844	0.46	0.00	7.42	0.00	2.02	0.00	0.90	0.00
135-7844	0.46	0.00	7.52	0.00	2.02	0.00	0.90	0.00
136-7844	0.46	0.00	7.42	0.00	2.02	0.00	0.90	0.00
137-7844	0.46	0.00	7.39	0.00	2.02	0.00	0.89	0.00
138-7844	0.46	0.00	7.42	0.00	2.02	0.00	0.90	0.00
139-7844	0.46	0.00	7.40	0.00	2.02	0.00	0.90	0.00
140-7844	0.46	0.00	7.39	0.00	2.02	0.00	0.90	0.00
141-7844	0.46	0.00	7.43	0.00	2.01	0.00	0.90	0.00
142-7844	0.46	0.00	7.39	0.00	2.02	0.00	0.90	0.00
143-7844	0.46	0.00	7.40	0.00	2.02	0.00	0.90	0.00
144-7844	0.46	0.00	7.41	0.00	2.02	0.00	0.89	0.00
145-7844	0.46	0.00	7.57	0.00	2.02	0.00	0.90	0.00
146-7844	0.45	0.00	7.40	0.00	2.03	0.00	0.89	0.00
147-7844	0.46	0.00	7.52	0.00	2.02	0.00	0.89	0.00
148-7844	0.46	0.00	7.45	0.00	2.03	0.00	0.90	0.00
149-7844	0.46	0.00	7.40	0.00	2.02	0.00	0.90	0.00
150-7844	0.46	0.00	[illegible]	0.00	2.02	[illegible]	0.90	0.00

TABLE A-I - BEFORE SUBGROUP C1 ACCEPTANCE TEST (Cont'd)

TEST DATA - XM587 INTERFACE HYBRID PAGE 2 OF 4

CONTRACT NO. SUBGROUP C-1 (57-MM GUNFIRE)

	+VP		IR14		V12		-VP	
NOTES	1	2	1	2	1	2	1	2
UNIT NO.-DATE CODE								
126-7844	29.05	0.00	1.08	0.00	-0.00	0.00	-29.03	0.00
127-7844	29.08	0.00	1.13	0.00	-0.00	0.00	-29.07	0.00
128-7844	28.98	0.00	1.12	0.00	-0.00	0.00	-29.05	0.00
129-7844	29.08	0.00	1.11	0.00	-0.00	0.00	-29.07	0.00
130-7844	29.06	0.00	1.29	0.00	-0.00	0.00	-29.05	0.00
131-7844	29.06	0.00	1.14	0.00	-0.00	0.00	-29.04	0.00
132-7844	29.03	0.00	1.19	0.00	-0.00	0.00	-29.02	0.00
133-7844	28.98	0.00	1.04	0.00	-0.00	0.00	-29.00	0.00
134-7844	29.07	0.00	1.16	0.00	-0.00	0.00	-29.04	0.00
135-7844	28.96	0.00	1.08	0.00	-0.00	0.00	-28.99	0.00
136-7844	29.07	0.00	1.34	0.00	-0.00	0.00	-29.05	0.00
137-7844	29.03	0.00	1.06	0.00	-0.00	0.00	-29.02	0.00
138-7844	29.11	0.00	1.15	0.00	-0.00	0.00	-29.05	0.00
139-7844	29.03	0.00	1.04	0.00	-0.00	0.00	-29.04	0.00
140-7844	29.05	0.00	1.06	0.00	-0.00	0.00	-29.04	0.00
141-7844	28.99	0.00	1.07	0.00	-0.00	0.00	-29.03	0.00
142-7844	28.98	0.00	1.04	0.00	-0.00	0.00	-29.02	0.00
143-7844	29.01	0.00	1.15	0.00	-0.00	0.00	-29.02	0.00
144-7844	29.07	0.00	1.25	0.00	-0.00	0.00	-29.05	0.00
145-7844	28.91	0.00	0.97	0.00	-0.00	0.00	-28.97	0.00
146-7844	29.08	0.00	1.11	0.00	-0.00	0.00	-29.06	0.00
147-7844	29.11	0.00	1.16	0.00	-0.00	0.00	-29.05	0.00
148-7844	29.11	0.00	1.21	0.00	-0.00	0.00	-29.05	0.00
149-7844	29.04	0.00	1.03	0.00	-0.00	0.00	-29.03	0.00
150-7844	29.09	0.00	1.13	0.00	-0.00	0.00	-29.06	0.00

TABLE A-I - BEFORE SUBGROUP C1 ACCEPTANCE TEST (Cont'd)

TEST DATA - [illegible] HYBRID — PAGE 3 OF 9

CONTRACT NO. — SUBGROUP C-1 (57-MM GUNFIRE)

	IR45		V2A		V2B		V1A	
NOTES	1	2	1	2	1	2	1	2
UNIT NO.-DATE CODE								
126-7844	-0.47	0.00	0.00	0.00	-9.45	0.00	-2.43	0.00
127-7844	-0.47	0.00	0.00	0.00	-9.43	0.00	-2.43	0.00
128-7844	-0.47	0.00	0.00	0.00	-9.42	0.00	-2.43	0.00
129-7844	-0.47	0.00	0.00	0.00	-9.54	0.00	-2.43	0.00
130-7844	-0.47	0.00	0.00	0.00	-9.53	0.00	-2.43	0.00
131-7844	-0.47	0.00	0.00	0.00	-9.53	0.00	-2.43	0.00
132-7844	-0.47	0.00	0.00	0.00	-9.52	0.00	-2.43	0.00
133-7844	-0.47	0.00	0.00	0.00	-8.92	0.00	-2.43	0.00
134-7844	-0.47	0.00	0.00	0.00	-9.55	0.00	-2.43	0.00
135-7844	-0.47	0.00	0.00	0.00	-8.53	0.00	-2.43	0.00
136-7844	-0.47	0.00	0.00	0.00	-9.52	0.00	-2.43	0.00
137-7844	-0.47	0.00	0.00	0.00	-9.41	0.00	-2.43	0.00
138-7844	-0.47	0.00	0.00	0.00	-9.45	0.00	-2.43	0.00
139-7844	-0.47	0.00	0.00	0.00	-8.70	0.00	-2.43	0.00
140-7844	-0.47	0.00	0.00	0.00	-9.41	0.00	-2.43	0.00
141-7844	-0.47	0.00	0.00	0.00	-9.41	0.00	-2.43	0.00
142-7844	-0.47	0.00	0.00	0.00	-9.39	0.00	-2.43	0.00
143-7844	-0.47	0.00	0.00	0.00	-9.52	0.00	-2.43	0.00
144-7844	-0.47	0.00	0.00	0.00	-9.61	0.00	-2.43	0.00
145-7844	-0.47	0.00	0.00	0.00	-8.81	0.00	-2.43	0.00
146-7844	-0.47	0.00	0.00	0.00	-9.53	0.00	-2.43	0.00
147-7844	-0.47	0.00	0.00	0.00	-9.45	0.00	-2.43	0.00
148-7844	-0.47	0.00	0.00	0.00	-9.56	0.00	-2.43	0.00
149-7844	-0.47	0.00	0.00	0.00	-8.50	0.00	-2.43	0.00
150-7844	-0.47	0.00	0.00	0.00	-9.56	0.00	-2.43	0.00

TABLE A-I - BEFORE SUBGROUP C1 ACCEPTANCE TEST (Cont'd)

TEST DATA - XM587 INTERFACE HYBRID PAGE 4 OF 9

CONTRACT NO. SUBGROUP C-1 (57-MM GUNFIRE)

	V1AD		IR39		V18		V1BD	
NOTES	1	2	1	2	1	2	1	2
UNIT NO.-DATE CODE								
126-7844	-3.78	0.00	-0.56	0.00	-15.41	0.00	-13.76	0.00
127-7844	-3.78	0.00	-0.57	0.00	-15.35	0.00	-13.71	0.00
128-7844	-3.77	0.00	-0.57	0.00	-15.35	0.00	-13.69	0.00
129-7844	-3.77	0.00	-0.56	0.00	-15.37	0.00	-13.70	0.00
130-7844	-3.78	0.00	-0.57	0.00	-15.33	0.00	-13.69	0.00
131-7844	-3.75	0.00	-0.56	0.00	-15.36	0.00	-13.70	0.00
132-7844	-3.77	0.00	-0.57	0.00	-15.33	0.00	-13.71	0.00
133-7844	-3.78	0.00	-0.57	0.00	-15.44	0.00	-13.81	0.00
134-7844	-3.78	0.00	-0.56	0.00	-15.32	0.00	-13.70	0.00
135-7844	-3.78	0.00	-0.57	0.00	-15.47	0.00	-13.81	0.00
136-7844	-3.77	0.00	-0.57	0.00	-15.27	0.00	-13.66	0.00
137-7844	-3.78	0.00	-0.57	0.00	-15.42	0.00	-13.77	0.00
138-7844	-3.78	0.00	-0.57	0.00	-15.33	0.00	-13.70	0.00
139-7844	-3.79	0.00	-0.57	0.00	-15.44	0.00	-13.80	0.00
140-7844	-3.77	0.00	-0.57	0.00	-15.42	0.00	-13.77	0.00
141-7844	-3.78	0.00	-0.57	0.00	-15.41	0.00	-13.76	0.00
142-7844	-3.76	0.00	-0.56	0.00	-15.43	0.00	-13.73	0.00
143-7844	-3.76	0.00	-0.56	0.00	-15.33	0.00	-13.67	0.00
144-7844	-3.76	0.00	-0.57	0.00	-15.30	0.00	-13.69	0.00
145-7844	-3.77	0.00	-0.57	0.00	-15.45	0.00	-13.79	0.00
146-7844	-3.78	0.00	-0.56	0.00	-15.37	0.00	-13.71	0.00
147-7844	-3.78	0.00	-0.57	0.00	-15.32	0.00	-13.70	0.00
148-7844	-3.78	0.00	-0.57	0.00	-15.28	0.00	-13.67	0.00
149-7844	-3.76	0.00	-0.57	0.00	-15.45	0.00	-13.80	0.00
150-7844	-3.78	0.00	-0.56	0.00	-15.35	0.00	-13.72	0.00

TABLE A-I - BEFORE SUBGROUP C1 ACCEPTANCE TEST (Cont'd)

TEST DATA. - XM587 INTERFACE HYBRID

CONTRACT NO. SUBGROUP C-1 (57-MM GUNFIRE)

	IR42		IR8		V11A		V10A	
NOTES	1	2	1	2	1	2	1	2
UNIT NO.-DATE CODE								
126-7844	-0.28	0.00	-2.47	0.00	-23.21	0.00	-24.05	0.00
127-7844	-0.28	0.00	-2.57	0.00	-22.30	0.00	-23.14	0.00
128-7844	-0.28	0.00	-2.60	0.00	-22.15	0.00	-22.99	0.00
129-7844	-0.28	0.00	-2.58	0.00	-22.14	0.00	-22.97	0.00
130-7844	-0.28	0.00	-2.58	0.00	-23.92	0.00	-24.77	0.00
131-7844	-0.28	0.00	-2.60	0.00	-23.52	0.00	-24.37	0.00
132-7844	-0.28	0.00	-2.66	0.00	-22.00	0.00	-22.84	0.00
133-7844	-0.28	0.00	-2.38	0.00	-23.78	0.00	-24.63	0.00
134-7844	-0.28	0.00	-2.76	0.00	-24.50	0.00	-25.35	0.00
135-7844	-0.28	0.00	-2.20	0.00	-23.36	0.00	-24.21	0.00
136-7844	-0.28	0.00	-2.74	0.00	-22.09	0.00	-22.93	0.00
137-7844	-0.28	0.00	-2.40	0.00	-23.16	0.00	-24.01	0.00
138-7844	-0.28	0.00	-2.68	0.00	-23.28	0.00	-24.13	0.00
139-7844	-0.28	0.00	-2.34	0.00	-23.00	0.00	-23.85	0.00
140-7844	-0.28	0.00	-2.45	0.00	-23.58	0.00	-24.42	0.00
141-7844	-0.28	0.00	-2.42	0.00	-23.37	0.00	-24.22	0.00
142-7844	-0.28	0.00	-2.41	0.00	-23.91	0.00	-24.75	0.00
143-7844	-0.28	0.00	-2.61	0.00	-22.24	0.00	-23.08	0.00
144-7844	-0.28	0.00	-2.67	0.00	-21.86	0.00	-22.70	0.00
145-7844	-0.28	0.00	-2.35	0.00	-23.64	0.00	-24.49	0.00
146-7844	-0.28	0.00	-3.27	0.00	-21.95	0.00	-22.79	0.00
147-7844	-0.28	0.00	-2.67	0.00	-23.35	0.00	-24.20	0.00
148-7844	-0.28	0.00	-3.79	0.00	-22.90	0.00	-23.75	0.00
149-7844	-0.28	0.00	-2.28	0.00	-23.07	0.00	-23.91	0.00
150-7844	-0.28	0.00	-2.58	0.00	-23.89	0.00	-24.74	0.00

TABLE A-I - BEFORE SUBGROUP C1 ACCEPTANCE TEST (Cont'd)

TEST DATA - XM587 INTERFACE HYBRID PAGE 6 OF 9

CONTRACT NO. SUBGROUP C-1 (57-MM GUNFIRE)

	V13A		V11B		V8A		V5A	
NOTES	1	2	1	2	1	2	1	2
UNIT NO.-DATE CODE								
126-7844	-0.00	0.00	-25.99	0.00	-0.00	0.00	0.00	0.00
127-7844	-0.00	0.00	-25.99	0.00	-0.00	0.00	0.00	0.00
128-7844	-0.00	0.00	-25.99	0.00	-0.00	0.00	0.00	0.00
129-7844	-0.00	0.00	-26.00	0.00	-0.00	0.00	0.00	0.00
130-7844	-0.00	0.00	-25.99	0.00	-0.00	0.00	0.00	0.00
131-7844	-0.00	0.00	-26.00	0.00	-0.00	0.00	0.00	0.00
132-7844	-0.00	0.00	-25.98	0.00	-0.00	0.00	0.00	0.00
133-7844	-0.00	0.00	-25.99	0.00	-0.00	0.00	0.00	0.00
134-7844	-0.00	0.00	-25.99	0.00	-0.00	0.00	0.00	0.00
135-7844	-0.00	0.00	-25.99	0.00	-0.00	0.00	0.00	0.00
136-7844	-0.00	0.00	-25.99	0.00	-0.00	0.00	0.00	0.00
137-7844	-0.00	0.00	-25.99	0.00	-0.00	0.00	0.00	0.00
138-7844	-0.00	0.00	-25.98	0.00	-0.00	0.00	0.00	0.00
139-7844	0.00	0.00	-25.99	0.00	-0.00	0.00	0.00	0.00
140-7844	-0.00	0.00	-25.99	0.00	-0.00	0.00	0.00	0.00
141-7844	-0.00	0.00	-25.98	0.00	-0.00	0.00	0.00	0.00
142-7844	-0.00	0.00	-25.99	0.00	-0.00	0.00	0.00	0.00
143-7844	-0.00	0.00	-25.99	0.00	-0.00	0.00	0.00	0.00
144-7844	-0.00	0.00	-25.99	0.00	-0.00	0.00	0.00	0.00
145-7844	-0.00	0.00	-25.98	0.00	-0.00	0.00	0.00	0.00
146-7844	-0.00	0.00	-26.00	0.00	-0.00	0.00	0.00	0.00
147-7844	-0.00	0.00	-25.99	0.00	-0.00	0.00	0.00	0.00
148-7844	-0.00	0.00	-25.98	0.00	-0.00	0.00	0.00	0.00
149-7844	-0.00	0.00	-25.99	0.00	-0.00	0.00	0.00	0.00
150-7844	-0.00	0.00	-26.00	0.00	-0.00	0.00	0.00	0.00

TABLE A-I - BEFORE SUBGROUP C1 ACCEPTANCE TEST (Cont'd)

TEST DATA - XM587 INTERFACE HYBRID PAGE 7 OF 9

CONTRACT NO. SUBGROUP C-1 (57-MM GUNFIRE)

	VSB		VSC		VSD		TSA	
NOTES	1	2	1	2	1	2	1	2
UNIT NO.-DATE CODE								
126-7844	-12.09	0.00	0.00	0.00	-12.75	0.00	18	0
127-7844	-12.35	0.00	0.00	0.00	-13.05	0.00	0	0
128-7844	-12.40	0.00	0.00	0.00	-11.98	0.00	27	0
129-7844	-12.32	0.00	0.00	0.00	-13.02	0.00	22	0
130-7844	-12.36	0.00	0.00	0.00	-13.01	0.00	18	0
131-7844	-12.23	0.00	0.00	0.00	-12.85	0.00	19	0
132-7844	-12.39	0.00	0.00	0.00	-12.69	0.00	18	0
133-7844	-11.98	0.00	0.00	0.00	-12.59	0.00	23	0
134-7844	-12.45	0.00	0.00	0.00	-13.12	0.00	18	0
135-7844	-11.93	0.00	0.00	0.00	-12.57	0.00	19	0
136-7844	-12.44	0.00	0.00	0.00	-12.67	0.00	20	0
137-7844	-11.96	0.00	0.00	0.00	-12.62	0.00	25	0
138-7844	-12.49	0.00	0.00	0.00	-12.09	0.00	21	0
139-7844	-11.92	0.00	0.00	0.00	-12.61	0.00	21	0
140-7844	-12.21	0.00	0.00	0.00	-12.82	0.00	31	0
141-7844	-12.02	0.00	0.00	0.00	-12.66	0.00	28	0
142-7844	-11.96	0.00	0.00	0.00	-12.59	0.00	51	0
143-7844	-12.38	0.00	0.00	0.00	-12.52	0.00	29	0
144-7844	-12.51	0.00	0.00	0.00	-12.62	0.00	41	0
145-7844	-11.82	0.00	0.00	0.00	-12.46	0.00	28	0
146-7844	-12.31	0.00	0.00	0.00	-11.99	0.00	19	0
147-7844	-12.52	0.00	0.00	0.00	-12.53	0.00	19	0
148-7844	-12.59	0.00	0.00	0.00	-12.68	0.00	31	0
149-7844	-11.92	0.00	0.00	0.00	-12.60	0.00	33	0
150-7844	-12.38	0.00	0.00	0.00	-13.05	0.00	11	0

TABLE A-I - BEFORE SUBGROUP C1 ACCEPTANCE TEST (Cont'd)

TEST DATA - X5587 INTERFACE HYBRID

CONTRACT NO. SUBGROUP C-1 (57-MM GUNFIRE)

	T5H		V7A		V8H		V7B	
NOTES	1	2	1	2	1	2	1	2
UNIT NO.-DATE CODE								
126-7844	42	0	-0.00	0.00	-16.96	0.00	-14.78	0.00
127-7844	36	0	-0.00	0.00	-16.96	0.00	-14.62	0.00
128-7844	37	0	-0.00	0.00	-16.96	0.00	-14.94	0.00
129-7844	38	0	-0.00	0.00	-16.96	0.00	-14.78	0.00
130-7844	38	0	-0.00	0.00	-16.96	0.00	-14.94	0.00
131-7844	40	0	-0.00	0.00	-16.96	0.00	-14.78	0.00
132-7844	37	0	-0.00	0.00	-16.96	0.00	-14.62	0.00
133-7844	41	0	-0.00	0.00	-16.96	0.00	-15.10	0.00
134-7844	35	0	-0.00	0.00	-16.96	0.00	-14.78	0.00
135-7844	43	0	-0.00	0.00	-16.96	0.00	-14.62	0.00
136-7844	36	0	-0.00	0.00	-16.96	0.00	-14.78	0.00
137-7844	43	0	-0.00	0.00	-16.96	0.00	-14.94	0.00
138-7844	37	0	-0.00	0.00	-16.96	0.00	-14.78	0.00
139-7844	42	0	0.00	0.00	-16.96	0.00	-14.94	0.00
140-7844	42	0	-0.00	0.00	-16.96	0.00	-14.78	0.00
141-7844	41	0	-0.00	0.00	-16.96	0.00	-14.47	0.00
142-7844	44	0	-0.00	0.00	-16.96	0.00	-14.78	0.00
143-7844	37	0	-0.00	0.00	-16.96	0.00	-14.94	0.00
144-7844	37	0	-0.00	0.00	-16.96	0.00	-14.78	0.00
145-7844	43	0	-0.00	0.00	-16.96	0.00	-14.94	0.00
146-7844	37	0	-0.00	0.00	-16.96	0.00	-14.78	0.00
147-7844	35	0	-0.00	0.00	-16.96	0.00	-14.94	0.00
148-7844	36	0	-0.00	0.00	-16.96	0.00	-14.78	0.00
149-7844	42	0	0.00	0.00	-16.96	0.00	-14.62	0.00
150-7844	35	0	-0.00	0.00	-16.96	0.00	-15.19	0.00

TABLE A-I - BEFORE SUBGROUP C1 ACCEPTANCE TEST (Cont'd)

TEST DATA - XM547 INTERFACE HYBRID PAGE 9 OF 9

CONTRACT NO. SUBGROUP C-1 (57-MM GUNFIRE)

	V7C	
NOTES	1	2
UNIT NO.-DATE CODE		
126-7844	-23.70	0.00
127-7844	-22.58	0.00
128-7844	-23.90	0.00
129-7844	-23.73	0.00
130-7844	-23.90	0.00
131-7844	-23.73	0.00
132-7844	-23.40	0.00
133-7844	-24.11	0.00
134-7844	-23.80	0.00
135-7844	-23.50	0.00
136-7844	-23.60	0.00
137-7844	-24.00	0.00
138-7844	-23.84	0.00
139-7844	-23.90	0.00
140-7844	-23.73	0.00
141-7844	-23.29	0.00
142-7844	-23.73	0.00
143-7844	-24.00	0.00
144-7844	-23.73	0.00
145-7844	-23.90	0.00
146-7844	-23.60	0.00
147-7844	-23.90	0.00
148-7844	-23.73	0.00
149-7844	-23.29	0.00
150-7844	-23.40	0.00

TABLE A-II - AFTER SUBGROUP C1 ACCEPTANCE TEST

TEST DATA - X3557 INTERFACE HYBRID

CONTRACT NO.

SUBGROUP C-1 (57-MM GUNFIRE)

LOT NO. 1

	IR6		IR10		IR16		IR3	
NOTES	1	2	1	2	1	2	1	2
UNIT NO.-DATE CODE								
126-7844	0.00	0.46	0.00	7.46	0.00	2.03	0.00	0.90
127-7844	0.00	0.46	0.00	7.51	0.00	2.03	0.00	0.89
128-7844	0.00	0.46	0.00	7.49	0.00	2.02	0.00	0.89
129-7844	0.00	0.46	0.00	7.48	0.00	2.02	0.00	0.89
130-7844	0.00	0.46	0.00	7.52	0.00	2.02	0.00	0.89
131-7844	0.00	0.46	0.00	7.46	0.00	2.03	0.00	0.89
132-7844	0.00	0.46	0.00	7.46	0.00	2.03	0.00	0.89
133-7844	0.00	0.46	0.00	7.47	0.00	2.02	0.00	0.90
134-7844	0.00	0.46	0.00	7.44	0.00	2.02	0.00	0.90
135-7844	0.00	0.46	0.00	7.50	0.00	2.02	0.00	0.89
136-7844	0.00	0.46	0.00	7.44	0.00	2.02	0.00	0.90
137-7844	0.00	0.46	0.00	7.53	0.00	2.02	0.00	0.89
138-7844	0.00	0.46	0.00	7.63	0.00	2.02	0.00	0.89
139-7844	0.00	0.45	0.00	7.50	0.00	2.03	0.00	0.89
140-7844	0.00	0.46	0.00	7.53	0.00	2.03	0.00	0.89
141-7844	0.00	0.46	0.00	7.46	0.00	2.02	0.00	0.89
142-7844	0.00	0.46	0.00	7.47	0.00	2.01	0.00	0.89
143-7844	0.00	0.46	0.00	7.47	0.00	2.02	0.00	0.90
144-7844	0.00	0.46	0.00	7.50	0.00	2.03	0.00	0.90
145-7844	0.00	0.46	0.00	7.51	0.00	2.02	0.00	0.90
146-7844	0.00	0.46	0.00	7.44	0.00	2.02	0.00	0.89
147-7844	0.00	0.46	0.00	7.50	0.00	2.02	0.00	0.90
148-7844	0.00	0.46	0.00	7.57	0.00	2.03	0.00	0.90
149-7844	0.00	0.46	0.00	7.49	0.00	2.03	0.00	0.89
150-7844	0.00	0.46	0.00	16.56	0.00	2.03	0.00	0.89

TABLE A-II - AFTER SUBGROUP C1 ACCEPTANCE TEST (Cont'd)

TEST DATA - XM557 INTERFACE HYBRID PAGE 2 OF 9

CONTRACT NO. SUBGROUP C-1 (57-M4 GUNFIRE)

	+VP		IR14		V12		-VP	
NOTES	1	2	1	2	1	2	1	2
UNIT NO.-DATE CODE								
126-7844	0.00	29.04	0.00	1.09	0.00	-0.00	0.00	-29.09
127-7844	0.00	29.02	0.00	1.08	0.00	-0.00	0.00	-29.06
128-7844	0.00	29.01	0.00	1.03	0.00	-0.00	0.00	-29.07
129-7844	0.00	29.06	0.00	1.13	0.00	-0.00	0.00	-29.09
130-7844	0.00	29.01	0.00	1.06	0.00	-0.00	0.00	-29.05
131-7844	0.00	29.05	0.00	1.21	0.00	-0.00	0.00	-29.07
132-7844	0.00	29.04	0.00	1.13	0.00	-0.00	0.00	-29.07
133-7844	0.00	29.04	0.00	1.15	0.00	-0.00	0.00	-29.08
134-7844	0.00	28.89	0.00	0.97	0.00	-0.00	0.00	-28.99
135-7844	0.00	29.05	0.00	1.20	0.00	-0.00	0.00	-29.07
136-7844	0.00	29.01	0.00	1.04	0.00	-0.00	0.00	-29.07
137-7844	0.00	29.09	0.00	1.15	0.00	-0.00	0.00	-29.08
138-7844	0.00	29.09	0.00	1.16	0.00	-0.00	0.00	-29.08
139-7844	0.00	29.06	0.00	1.11	0.00	-0.00	0.00	-29.10
140-7844	0.00	28.99	0.00	1.15	0.00	-0.00	0.00	-29.05
141-7844	0.00	28.96	0.00	1.04	0.00	-0.00	0.00	-29.05
142-7844	0.00	28.97	0.00	1.06	0.00	-0.00	0.00	-29.05
143-7844	0.00	29.03	0.00	1.06	0.00	-0.00	0.00	-29.07
144-7844	0.00	28.95	0.00	1.02	0.00	-0.00	0.00	-29.03
145-7844	0.00	29.09	0.00	1.15	0.00	-0.00	0.00	-29.09
146-7844	0.00	29.06	0.00	1.12	0.00	-0.00	0.00	-29.10
147-7844	0.00	28.96	0.00	1.12	0.00	-0.00	0.00	-29.08
148-7844	0.00	28.94	0.00	1.01	0.00	-0.00	0.00	-29.02
149-7844	0.00	29.05	0.00	1.16	0.00	-0.00	0.00	-29.07
150-7844	0.00	26.98	0.00	5.86	0.00	-0.99	0.00	-16.40

TABLE A-II - AFTER SUBGROUP C1 ACCEPTANCE TEST (Cont'd)

TEST DATA - XM587 INTERFACE HYBRID PAGE 5 OF 9

CONTRACT NO. SUBGROUP C-1 (57-MM GUNFIRE)

	IR45		V2A		V2B		V1A	
NOTES	1	2	1	2	1	2	1	2
UNIT NO.-DATE CODE								
126-7844	0.00	-0.47	0.00	0.00	0.00	-9.49	0.00	-2.43
127-7844	0.00	-0.47	0.00	0.00	0.00	-9.47	0.00	-2.43
128-7844	0.00	-0.47	0.00	0.00	0.00	-8.51	0.00	-2.43
129-7844	0.00	-0.47	0.00	0.00	0.00	-9.58	0.00	-2.43
130-7844	0.00	-0.47	0.00	0.00	0.00	-9.43	0.00	-2.43
131-7844	0.00	-0.47	0.00	0.00	0.00	-9.55	0.00	-2.43
132-7844	0.00	-0.47	0.00	0.00	0.00	-9.56	0.00	-2.43
133-7844	0.00	-0.47	0.00	0.00	0.00	-9.56	0.00	-2.43
134-7844	0.00	-0.47	0.00	0.00	0.00	-8.85	0.00	-2.43
135-7844	0.00	-0.47	0.00	0.00	0.00	-9.64	0.00	-2.43
136-7844	0.00	-0.47	0.00	0.00	0.00	-8.65	0.00	-2.43
137-7844	0.00	-0.47	0.00	0.00	0.00	-9.48	0.00	-2.43
138-7844	0.00	-0.47	0.00	0.00	0.00	-9.48	0.00	-2.43
139-7844	0.00	-0.47	0.00	0.00	0.00	-9.55	0.00	-2.43
140-7844	0.00	-0.47	0.00	0.00	0.00	-9.53	0.00	-2.43
141-7844	0.00	-0.46	0.00	0.00	0.00	-9.39	0.00	-2.43
142-7844	0.00	-0.47	0.00	0.00	0.00	-9.42	0.00	-2.43
143-7844	0.00	-0.47	0.00	0.00	0.00	-9.46	0.00	-2.43
144-7844	0.00	-0.47	0.00	0.00	0.00	-8.91	0.00	-2.43
145-7844	0.00	-0.46	0.00	0.00	0.00	-9.56	0.00	-2.43
146-7844	0.00	-0.47	0.00	0.00	0.00	-9.56	0.00	-2.43
147-7844	0.00	-0.47	0.00	0.00	0.00	-9.44	0.00	-2.43
148-7844	0.00	-0.47	0.00	0.00	0.00	-8.48	0.00	-2.43
149-7844	0.00	-0.47	0.00	0.00	0.00	-9.58	0.00	-2.43
150-7844	0.00	-0.90	0.00	-0.00	0.00	-6.30	0.00	-9.90

TABLE A-II - AFTER SUBGROUP C1 ACCEPTANCE TEST (Cont'd)

TEST DATA - X3587 INTERFACE HYBRID - PAGE 4 OF 9

CONTRACT NO. . SUBGROUP C-1 (57-[illegible] GUNFIRE)

	V1AO		IR39		V1B		V1BO	
NOTES	1	2	1	2	1	2	1	2
UNIT NO.-DATE CODE								
126-7844	0.00	-3.77	0.00	-0.56	0.00	-15.41	0.00	-13.72
127-7844	0.00	-3.78	0.00	-0.56	0.00	-15.42	0.00	-13.77
128-7844	0.00	-3.78	0.00	-0.57	0.00	-15.46	0.00	-13.81
129-7844	0.00	-3.78	0.00	-0.56	0.00	-15.36	0.00	-13.73
130-7844	0.00	-3.78	0.00	-0.56	0.00	-15.43	0.00	-13.78
131-7844	0.00	-3.75	0.00	-0.57	0.00	-15.28	0.00	-13.67
132-7844	0.00	-3.75	0.00	-0.56	0.00	-15.37	0.00	-13.71
133-7844	0.00	-3.78	0.00	-0.57	0.00	-15.35	0.00	-13.70
134-7844	0.00	-3.77	0.00	-0.56	0.00	-15.46	0.00	-13.81
135-7844	0.00	-3.78	0.00	-0.56	0.00	-15.31	0.00	-13.70
136-7844	0.00	-3.78	0.00	-0.56	0.00	-15.45	0.00	-13.82
137-7844	0.00	-3.78	0.00	-0.57	0.00	-15.34	0.00	-13.71
138-7844	0.00	-3.78	0.00	-0.57	0.00	-15.34	0.00	-13.71
139-7844	0.00	-3.78	0.00	-0.56	0.00	-15.38	0.00	-13.72
140-7844	0.00	-3.76	0.00	-0.56	0.00	-15.35	0.00	-13.68
141-7844	0.00	-3.76	0.00	-0.56	0.00	-15.44	0.00	-13.75
142-7844	0.00	-3.77	0.00	-0.56	0.00	-15.42	0.00	-13.77
143-7844	0.00	-3.78	0.00	-0.57	0.00	-15.43	0.00	-13.78
144-7844	0.00	-3.77	0.00	-0.57	0.00	-15.45	0.00	-13.82
145-7844	0.00	-3.78	0.00	-0.56	0.00	-15.34	0.00	-13.69
146-7844	0.00	-3.77	0.00	-0.56	0.00	-15.37	0.00	-13.71
147-7844	0.00	-3.78	0.00	-0.57	0.00	-15.36	0.00	-13.70
148-7844	0.00	-3.78	0.00	-0.57	0.00	-15.47	0.00	-13.82
149-7844	0.00	-3.78	0.00	-0.56	0.00	-15.33	0.00	-13.70
150-7844	0.00	-9.98	0.00	-0.57	0.00	-26.95	0.00	-26.95

TABLE A-II - AFTER SUBGROUP C1 ACCEPTANCE TEST (Cont'd)

TEST DATA - XM587 INTERFACE HYBRID — PAGE 5 OF 9

CONTRACT NO. — SUBGROUP C-1 (57-MM GUNFIRE)

	IR42		IRB		V11A.		V10A	
NOTES	1	2	1	2	1	2	1	2
UNIT NO.-DATE CODE								
126-7844	0.00	-0.27	0.00	-3.70	0.00	-23.65	0.00	-24.49
127-7844	0.00	-0.28	0.00	-2.48	0.00	-23.21	0.00	-24.06
128-7844	0.00	-0.28	0.00	-2.29	0.00	-23.18	0.00	-24.02
129-7844	0.00	-0.28	0.00	-2.58	0.00	-23.93	0.00	-24.78
130-7844	0.00	-0.28	0.00	-2.42	0.00	-23.19	0.00	-24.04
131-7844	0.00	-0.28	0.00	-2.76	0.00	-22.09	0.00	-22.93
132-7844	0.00	-0.28	0.00	-2.61	0.00	-23.56	0.00	-24.40
133-7844	0.00	-0.28	0.00	-2.58	0.00	-23.92	0.00	-24.76
134-7844	0.00	-0.28	0.00	-2.35	0.00	-23.72	0.00	-24.56
135-7844	0.00	-0.29	0.00	-2.67	0.00	-21.85	0.00	-22.69
136-7844	0.00	-0.28	0.00	-2.35	0.00	-23.14	0.00	-23.98
137-7844	0.00	-0.28	0.00	-2.69	0.00	-23.30	0.00	-24.15
138-7844	0.00	-0.28	0.00	-2.13	0.00	-23.38	0.00	-24.23
139-7844	0.00	-0.28	0.00	-3.26	0.00	-21.95	0.00	-22.79
140-7844	0.00	-0.28	0.00	-2.62	0.00	-22.28	0.00	-23.12
141-7844	0.00	-0.28	0.00	-2.41	0.00	-23.92	0.00	-24.76
142-7844	0.00	-0.28	0.00	-2.43	0.00	-23.43	0.00	-24.28
143-7844	0.00	-0.28	0.00	-2.46	0.00	-23.57	0.00	-24.42
144-7844	0.00	-0.28	0.00	-2.39	0.00	-23.89	0.00	-24.73
145-7844	0.00	-0.28	0.00	-2.71	0.00	-23.53	0.00	-24.37
146-7844	0.00	-0.28	0.00	-2.59	0.00	-22.15	0.00	-23.00
147-7844	0.00	-0.28	0.00	-2.60	0.00	-22.17	0.00	-23.01
148-7844	0.00	-0.28	0.00	-2.21	0.00	-23.45	0.00	-24.30
149-7844	0.00	-0.28	0.00	-2.76	0.00	-24.45	0.00	-25.30
150-7844	0.00	-3.40	0.00	-6.65	0.00	-22.69	0.00	-23.74

TABLE A-II - AFTER SUBGROUP C1 ACCEPTANCE TEST (Cont'd)

TEST DATA - XH567 INTERFACE HYBRID

CONTRACT NO. SUBGROUP C-1 (57-MM GUNFIRE)

	V13A		V11B		V8A		V5A	
NOTES	1	2	1	2	1	2	1	2
UNIT NO.-DATE CODE								
126-7844	0.00	-0.00	0.00	-26.02	0.00	-0.00	0.00	0.00
127-7844	0.00	-0.00	0.00	-26.02	0.00	-0.00	0.00	0.00
128-7844	0.00	-0.00	0.00	-26.01	0.00	-0.00	0.00	0.00
129-7844	0.00	-0.00	0.00	-26.02	0.00	-0.00	0.00	0.00
130-7844	0.00	-0.00	0.00	-26.01	0.00	-0.00	0.00	0.00
131-7844	0.00	-0.00	0.00	-26.02	0.00	-0.00	0.00	0.00
132-7844	0.00	-0.00	0.00	-26.02	0.00	-0.00	0.00	0.00
133-7844	0.00	-0.00	0.00	-26.02	0.00	-0.00	0.00	0.00
134-7844	0.00	-0.00	0.00	-26.01	0.00	-0.00	0.00	-0.99
135-7844	0.00	-0.00	0.00	-26.02	0.00	-0.00	0.00	0.00
136-7844	0.00	-0.00	0.00	-26.02	0.00	-0.00	0.00	0.00
137-7844	0.00	-0.00	0.00	-26.01	0.00	-0.00	0.00	0.00
138-7844	0.00	-0.00	0.00	-0.82	0.00	-0.00	0.00	0.00
139-7844	0.00	-0.00	0.00	-26.02	0.00	-0.00	0.00	0.00
140-7844	0.00	-0.00	0.00	-26.01	0.00	-0.00	0.00	0.00
141-7844	0.00	-0.00	0.00	-26.01	0.00	-0.00	0.00	0.00
142-7844	0.00	-0.00	0.00	-26.01	0.00	-0.00	0.00	0.00
143-7844	0.00	-0.00	0.00	-26.01	0.00	-0.00	0.00	0.00
144-7844	0.00	-0.00	0.00	-26.01	0.00	-0.00	0.00	-0.99
145-7844	0.00	-0.00	0.00	-26.01	0.00	-0.00	0.00	0.00
146-7844	0.00	-0.00	0.00	-26.02	0.00	-0.00	0.00	0.00
147-7844	0.00	-0.00	0.00	-26.02	0.00	-0.00	0.00	0.00
148-7844	0.00	-0.00	0.00	-26.01	0.00	-0.00	0.00	0.00
149-7844	0.00	-0.00	0.00	-26.01	0.00	-0.00	0.00	0.00
150-7844	0.00	-0.00	0.00	-25.97	0.00	-0.00	0.00	-0.00

TABLE A-II - AFTER SUBGROUP C1 ACCEPTANCE TEST (Cont'd)

TEST DATA - XM587 INTERFACE HYBRID . PAGE 7 OF 9

CONTRACT NO. SUBGROUP C-1 (57-MM GUNFIRE)

	VSB		VSC		VSQ		TSA	
NOTES	1	2	1	2	1	2	1	2
UNIT NO.-DATE CODE								
126-7844	0.00	-12.22	0.00	0.00	0.00	-12.91	0	18
127-7844	0.00	-12.07	0.00	0.00	0.00	-12.77	0	16
128-7844	0.00	-11.89	0.00	0.00	0.00	-12.62	0	36
129-7844	0.00	-12.36	0.00	0.00	0.00	-13.08	0	12
130-7844	0.00	-11.94	0.00	0.00	0.00	-12.63	0	23
131-7844	0.00	-12.42	0.00	0.00	0.00	-12.67	0	21
132-7844	0.00	-12.21	0.00	0.00	0.00	-12.67	0	17
133-7844	0.00	-12.34	0.00	0.00	0.00	-13.03	0	18
134-7844	0.00	-11.36	0.00	-0.99	0.00	-11.96	0	0
135-7844	0.00	-12.50	0.00	0.00	0.00	-12.60	0	39
136-7844	0.00	-11.87	0.00	0.00	0.00	-12.62	0	6
137-7844	0.00	-12.47	0.00	0.00	0.00	-12.11	0	33
138-7844	0.00	-0.01	0.00	0.00	0.00	-0.01	0	0
139-7844	0.00	-12.28	0.00	0.00	0.00	-11.96	0	20
140-7844	0.00	-12.35	0.00	0.00	0.00	-12.54	0	31
141-7844	0.00	-11.92	0.00	0.00	0.00	-12.61	0	50
142-7844	0.00	-12.01	0.00	0.00	0.00	-12.68	0	6
143-7844	0.00	-12.20	0.00	0.00	0.00	-12.85	0	34
144-7844	0.00	-11.44	0.00	-0.99	0.00	-12.08	0	0
145-7844	0.00	-12.50	0.00	0.00	0.00	-12.59	0	37
146-7844	0.00	-12.30	0.00	0.00	0.00	-13.03	0	18
147-7844	0.00	-12.39	0.00	0.00	0.00	-11.99	0	24
148-7844	0.00	-11.90	0.00	0.00	0.00	-12.58	0	20
149-7844	0.00	-12.43	0.00	0.00	0.00	-13.14	0	18
150-7844	0.00	-12.57	0.00	-0.00	0.00	-12.68	0	30

TABLE A-II - AFTER SUBGROUP C1 ACCEPTANCE TEST (Cont'd)

TEST DATA - XM587 INTERFACE HYBRID PAGE 8 OF 9

CONTRACT NO. SUBGROUP C-1 (57-MM GUNFIRE)

	T5B		V7A		V8B		V7B	
NOTES	1	2	1	2	1	2	1	2
UNIT NO.-DATE CODE								
126-7844	0	38	0.00	-0.00	0.00	-16.98	0.00	-11.28
127-7844	0	41	0.00	-0.00	0.00	-16.98	0.00	-11.15
128-7844	0	42	0.00	-0.00	0.00	-16.96	0.00	-11.15
129-7844	0	34	0.00	-0.00	0.00	-16.98	0.00	-11.42
130-7844	0	41	0.00	-0.00	0.00	-16.98	0.00	-11.28
131-7844	0	36	0.00	-0.00	0.00	-16.96	0.00	-11.28
132-7844	0	40	0.00	-0.00	0.00	-16.98	0.00	-11.42
133-7844	0	38	0.00	-0.00	0.00	-16.98	0.00	-11.42
134-7844	0	0	0.00	-0.00	0.00	-16.98	0.00	-11.28
135-7844	0	36	0.00	-0.00	0.00	-16.98	0.00	-11.82
136-7844	0	0	0.00	-0.00	0.00	-16.98	0.00	-11.42
137-7844	0	36	0.00	-0.00	0.00	-16.98	0.00	-11.42
138-7844	0	0	0.00	-0.00	0.00	-16.98	0.00	-11.42
139-7844	0	37	0.00	-0.00	0.00	-16.98	0.00	-11.15
140-7844	0	37	0.00	-0.00	0.00	-16.98	0.00	-11.28
141-7844	0	44	0.00	-0.00	0.00	-16.98	0.00	-11.28
142-7844	0	0	0.00	-0.00	0.00	-16.98	0.00	-10.88
143-7844	0	41	0.00	-0.00	0.00	-16.98	0.00	-11.42
144-7844	0	0	0.00	-0.00	0.00	-16.98	0.00	-11.28
145-7844	0	36	0.00	-0.00	0.00	-16.98	0.00	-11.42
146-7844	0	37	0.00	-0.00	0.00	-16.98	0.00	-11.55
147-7844	0	37	0.00	-0.00	0.00	-16.98	0.00	-11.42
148-7844	0	43	0.00	-0.00	0.00	-16.98	0.00	-11.15
149-7844	0	35	0.00	-0.00	0.00	-16.98	0.00	-11.28
150-7844	0	36	0.00	-0.00	0.00	-16.98	0.00	-11.42

TABLE A-II - AFTER SUBGROUP C1 ACCEPTANCE TEST (Cont'd)

TEST DATA - XM587 INTERFACE HYBRID PAGE 9 OF 9

CONTRACT NO. SUBGROUP C-1 (57-MM GUNFIRE)

	V7C	
NOTES	1	2
UNIT NO.-DATE CODE		
126-7844	0.00	-18.22
127-7844	0.00	-18.09
128-7844	0.00	-18.09
129-7844	0.00	-18.33
130-7844	0.00	-18.19
131-7844	0.00	-18.30
132-7844	0.00	-18.44
133-7844	0.00	-18.30
134-7844	0.00	-18.19
135-7844	0.00	-19.01
136-7844	0.00	-18.30
137-7844	0.00	-18.33
138-7844	0.00	-18.50
139-7844	0.00	-18.09
140-7844	0.00	-18.19
141-7844	0.00	-18.35
142-7844	0.00	-15.58
143-7844	0.00	-18.22
144-7844	0.00	-18.19
145-7844	0.00	-18.33
146-7844	0.00	-18.55
147-7844	0.00	-18.40
148-7844	0.00	-18.09
149-7844	0.00	-18.19
150-7844	0.00	-18.22

APPENDIX B. PHASE IV - PILOT PRODUCTION LOT TRAVELERS

This appendix consists of tables B-I through B-IV, which are the actual phase IV travelers consolidated into four shipping lots numbered 7928, 7932, 7932R, and 7941.

TABLE B-I. SHIPPING LOT NUMBER (DATE CODE) 7928

Assembly Operations	Start Date	Quantity			
		Start	Sample	Reject	Accept
Apply Solder Paste	03/17/79	1536	0	0	1536
Mount Cap. SCR Ass'y	04/02/79	1536	0	0	1536
Reflow Solder	04/03/79	1536	0	0	1536
Remove Flux	04/03/79	1536	0	0	1536
Freon Clean	04/03/79	1536	0	0	1536
Epoxy Mount.IC/Cure	04/04/79	1536	0	0	1536
100% Visual Inspect	04/05/79	1536	0	0	1536
Quality Control Inspect	04/10/79	1536	3	10	1523
Cobehn Spray Clean	05/07/79	1523	0	0	1523
Wire Bond	05/07/79	1523	0	67	1456
100% Visual Inspect	05/09/79	1456	0	0	1456
100% Electrical Test	05/23/79	1456	0	898	558
Quality Control Inspect	05/23/79	558	0	0	558
Epoxy Coat Wires/Cure	05/23/79	558	0	0	558
Prepare Lead Frame Strip	03/17/79	558	0	0	558
Mount Sub. to Lead Frame	06/01/79	558	0	2	556
Apply Solder Paste	06/05/79	556	0	0	556
Reflow Solder	06/05/79	556	0	12	544
Remove Flux	06/05/79	544	0	0	544
Quality Control Inspect	06/25/79	544	0	7	537
Pack for Shipment	07/02/79	537	0	0	537
Transfer Mold*	07/09/79	537	0	59	478
Cut and Form Leads	07/19/79	478	0	1	477
Mark and Cure	07/23/79	477	0	7	470
Final Electrical Test	07/24/79	470	0	107	363
Quality Control Inspect**	10/26/79	363	0	64	299
Comparison Sample	09/12/79	12	0	0	12
Acceptance Sample	-	0	0	0	0
Pilot Lot Balance	10/30/79	-	-	-	289
Pack for Delivery	10/30/79	-	-	-	301
Total Shipment	10/30/79	-	-	-	301

Note: This is a consolidation of substrate assembly sublots HD001 through HD004 which were processed from substrate fabrication trimming lot B2 into mold lot one.

*Fifty nine true mold void rejects from mold lot one.

**Sixty four red lead known mechanical rejections.

TABLE B-II. SHIPPING LOT NUMBER (DATE CODE) 7932

Assembly Operations	Start Date	Quantity			
		Start	Sample	Reject	Accept
Apply Solder Paste	04/02/79	845	0	0	845
Mount Cap. SCR Ass'y	04/03/79	845	0	15	830
Reflow Solder	04/03/79	830	0	0	830
Remove Flux	04/03/79	830	0	0	830
Freon Clean	04/03/79	830	0	0	830
Epoxy Mount IC/Cure	04/04/79	830	0	5	825
100% Visual Inspect	04/05/79	825	0	173	652
Quality Control Inspect		652	0	0	652
Cobehn Spray Clean	05/24/79	652	0	0	652
Wire Bond	05/25/79	652	0	0	652
100% Visual Inspect	05/27/79	652	0	0	652
100% Electrical Test	05/30/79	652	0	233	419
Quality Control Inspect	06/01/79	419	0	3	416
Epoxy Coat Wires/Cure	07/03/79	416	0	0	416
Prepare Lead Frame Strip	04/02/79	416	0	0	416
Mount Sub. to Lead Frame	07/07/79	416	0	0	416
Apply Solder Paste	07/12/79	416	0	2	414
Reflow Solder	07/12/79	414	0	2	412
Remove Flux	07/12/79	412	0	0	412
Quality Control Inspect	07/16/79	412	0	0	413
Pack for Shipment	07/17/79	413	0	0	413
Transfer Mold*	08/06/79	413	0	141	272
Cut and Form Leads	08/08/79	272	0	0	272
Mark and Cure	08/09/79	272	0	0	272
Final Electrical Test	08/10/79	272	0	17	255
Quality Control Inspect	08/10/79	255	0	0	255
Comparison Sample	09/12/79	13	0	0	13
Acceptance Sample	10/30/79	158	0	16	158
Pilot Lot Balance	10/30/79	-	-	-	92
Pack for Delivery	10/30/79	-	-	-	263
Total Shipment	10/30/79	-	-	16	263

Note: This is a consolidation of substrate assembly sublots HD005 and HD006 which were processed from substrate fabrication trimming lot B1 into mold lot two.

*One true mold void reject plus 140 so-called SSD mold rejects from mold lot two.

TABLE B-III. SHIPPING LOT NUMBER (DATE CODE) 7932R

Assembly Operations	Start Date	Quantity			
		Start	Sample	Reject	Accept
Apply Solder Paste					
Mount Cap. SCR Ass'y					
Reflow Solder					
Remove Flux					
Freon Clean					
Epoxy Mount IC/Cure					
100% Visual Inspect*					
Quality Control Inspect		395	0	0	395
Cobehn Spray Clean	06/06/79	185	0	0	185
Wire Bond	06/06/79	185	0	0	185
100% Visual Inspect	06/07/79	185	0	0	185
100% Electrical Test	06/22/79	185	0	69	116
Quality Control Inspect	06/25/79	116	0	2	114
Epoxy Coat Wire/Cure	07/03/79	114	0	0	114
Prepare Lead Frame Strip	04/02/79	114	0	0	114
Mount Sub. to Lead Frame	07/05/79	114	0	0	114
Apply Solder Paste	07/13/79	114	0	0	114
Reflow Solder	07/13/79	114	0	0	114
Remove Flux	07/13/79	114	0	0	114
Quality Control Inspect	07/16/79	114	0	0	114
Pack for Shipment	07/16/79	114	0	0	114
Transfer Mold**	08/06/79	114	0	35	79
Cut and Form Leads	08/08/79	79	0	0	79
Mark and Cure	08/10/79	79	0	0	79
Final Electrical Test	08/10/79	79	0	3	76
Quality Control Inspect	08/10/79	76	0	0	76
Comparison Sample	-	0	0	0	0
Acceptance Sample	-	0	0	0	0
Pilot Lot Balance	10/30/79	-	-	-	77
Pack for Delivery	10/30/79	-	-	-	77
Total Shipment					

*These are the 395 units that were inadventently damaged by burnishing and became candidates for rework by replacement of components. Only 185 units were actually reworked in the unsegregated assembly rework sublot HDR01 and mold lot two.

**Thirty-five so-called SSD mold rejects from mold lot two.

TABLE B-IV. SHIPPING LOT NUMBER (DATE CODE) 7941

Assembly Operations	Start Date	Quantity			
		Start	Sample	Reject	Accept
Apply Solder Paste					
Mount Cap. SCR Ass'y					
Reflow Solder					
Remove Flux					
Freon Clean					
Epoxy Mount IC/Cure					
100% Visual Inspect					
Quality Control Inspect					
Cobehn Spray Clean					
Wire Bond					
100% Visual Inspect				267*	
100% Electrical Test	09/18/79	267	0	51	216
Quality Control Inspect	09/18/79	216	0	72	144
Epoxy Coat Wires/Cure					
Prepare Lead Frame Strip					
Mount Sub. to Lead Frame					
Apply Solder Paste					
Reflow Solder					
Remove Flux					
Quality Control Inspect					
Pack for Shipment					
Transfer Mold					
Cut and Form Leads					
Mark and Cure	10/10/79	144	0	0	144
Final Electrical Test	10/18/79	144	0	10	134
Quality Control Inspect	10/18/79	134	0	0	134
Comparison Sample	-	0	0	0	0
Acceptance Sample	-	0	0	0	0
Pilot Lot Balance	10/30/79	-	-	-	134
Pack for Delivery	10/30/79	-	-	-	134
Total Shipment	10/30/79	-	-	-	134

*These are the 267 mold rejections. Two hundred eight units were inadvertently classified as the so-called SSD mold rejects, and 49 units are true mold void rejects. Some of the true mold void rejects were electrically acceptable units at first electrical test. Eleven of the true mold void rejects were furnished to HDL on 9.17/79 as rejected units with data.

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